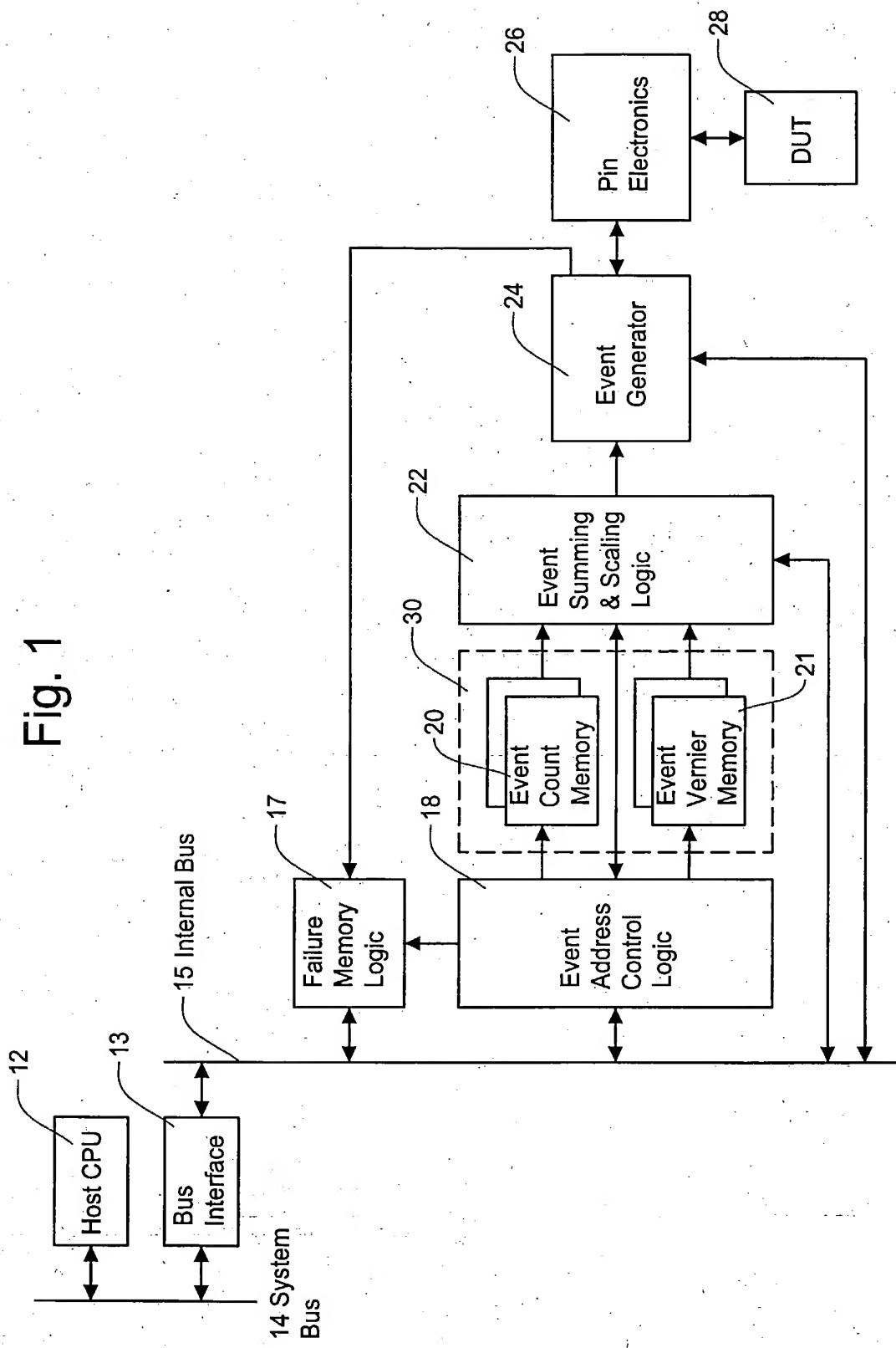


Fig. 1



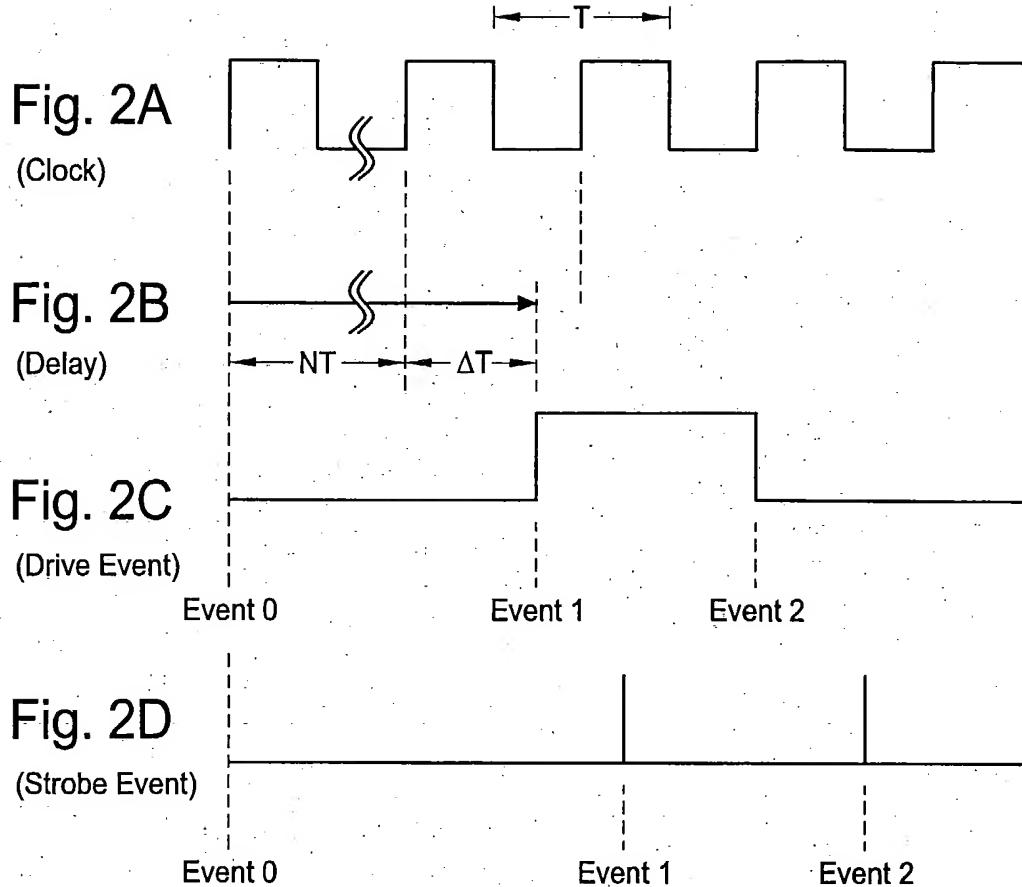


Fig. 3

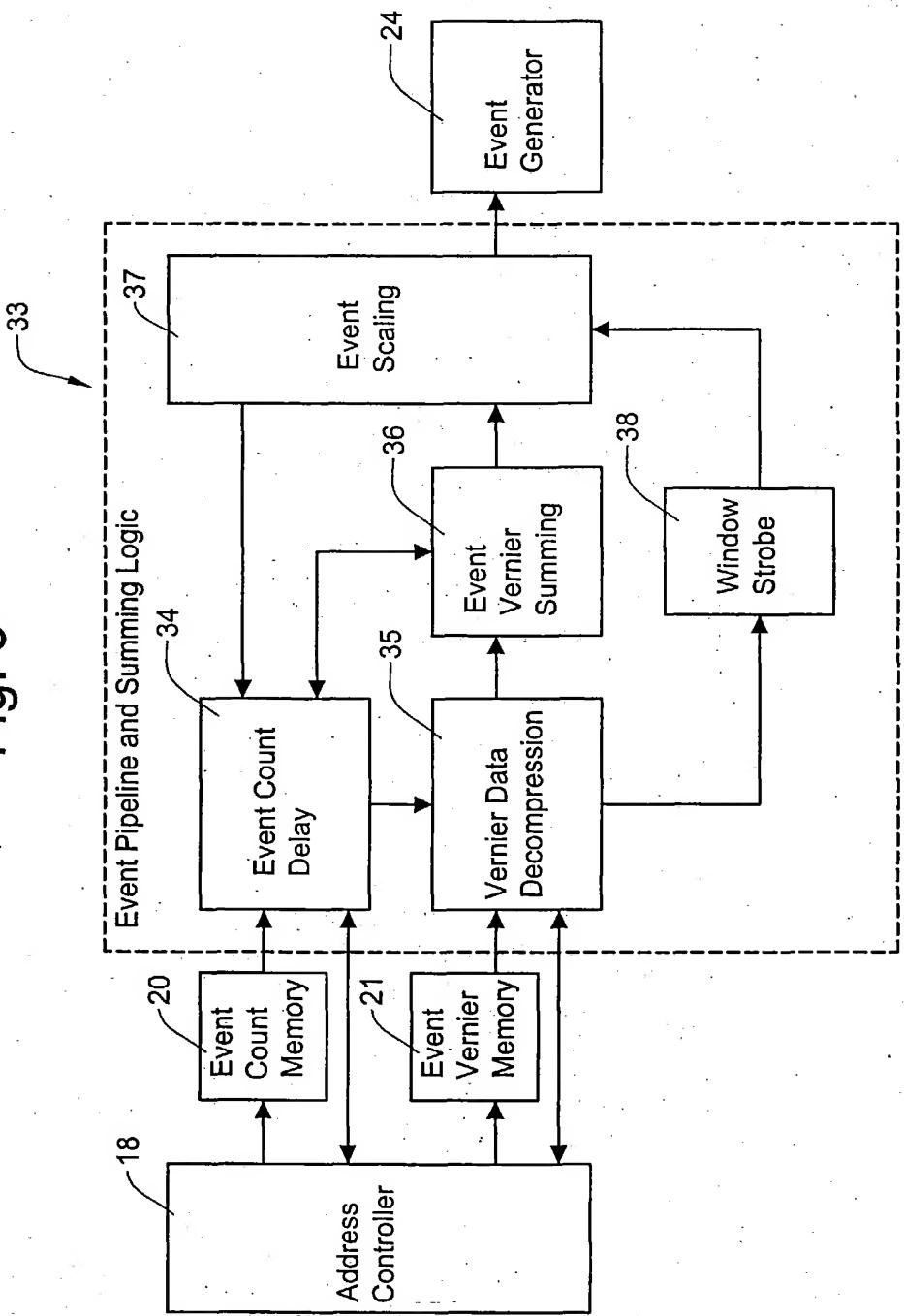


Fig. 4A

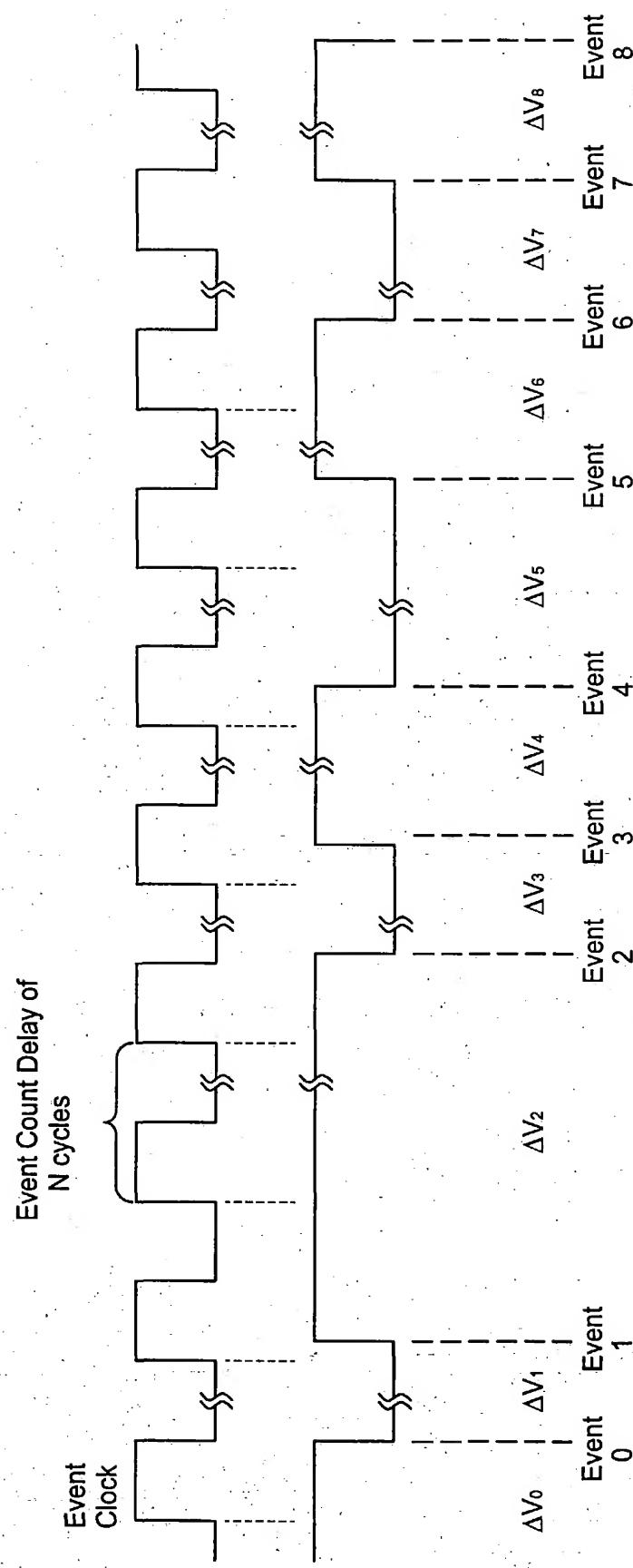


Fig. 4B

Event	Event Count	Event Vernier	Event Type
E0	C0	V0	Drive Low
E1	C1	V1	Drive High
E2	C2	V2	Drive Low
E3	C3	V3	Drive High
E4	C4	V4	Drive Low
E5	C5	V5	Drive High
E6	C6	V6	Drive Low
E7	C7	V7	Drive High
E8	C8	V8	Drive Low

Fig. 5

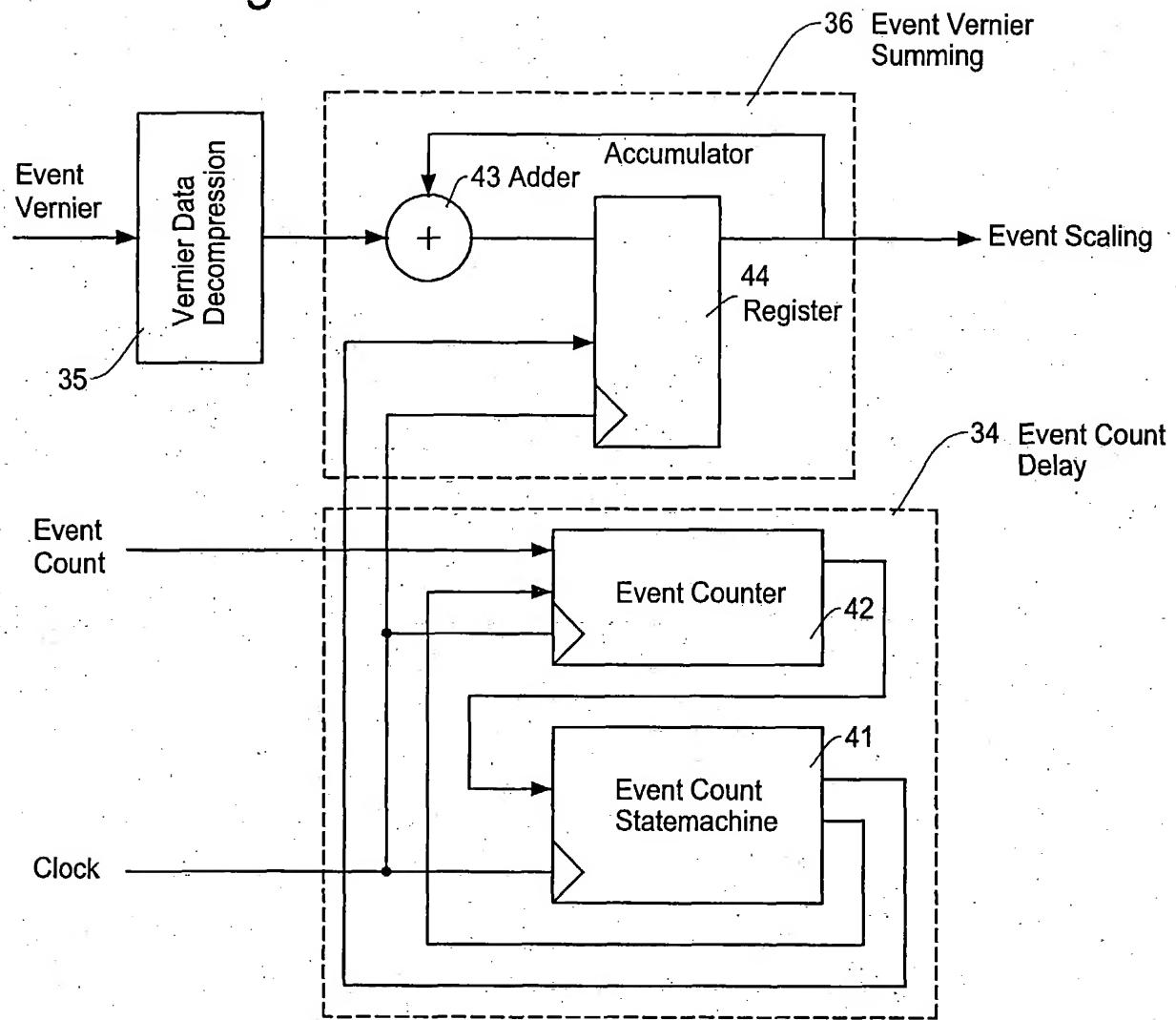


Fig. 6A

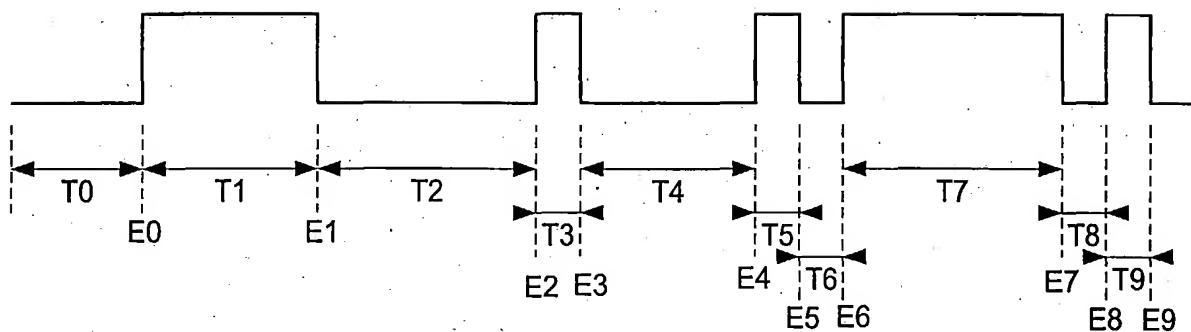


Fig. 6B

Event	Event Count Data	Event Vernier Data
E0	T0 count data	T0 vernier
E1	T1 count data	T1 vernier
E2	T2 count data	T2 vernier
E3	T3 count data	T3 vernier
E4	T4 count data	T4 vernier
E5	T5 count data	T5 vernier
E6	T6 count data	T6 vernier
E7	T7 count data	T7 vernier
E8	T8 count data	T8 vernier
E9	T9 count data	T9 vernier

Fig. 6C

Event	Event Count Memory	Event Vernier Memory
E0	T0 count data (Word 0)	0, 0, 0, T0 vernier
E1	T1 count data (Word 0)	0, T2 vernier, 0, T1 vernier
	T1 count data (Word 1)	T4 vernier, 0, 0, T3 vernier
E2, E3	T2 count data (Word 0)	0, 0, T6 vernier, T5 vernier
	T2 count data (Word 1)	0, T9 vernier, T8 vernier, T7 vernier
	T2 count data (Word 2)	(next vernier data)
E4, E5, E6	T4 count data (Word 0)	(next vernier data)
	T4 count data (Word 1)	(next vernier data)
	T4 count data (Word 2)	(next vernier data)
	T4 count data (Word 3)	(next vernier data)
E7, E8, E9	T7 count data (Word 0)	(next vernier data)

Fig. 7

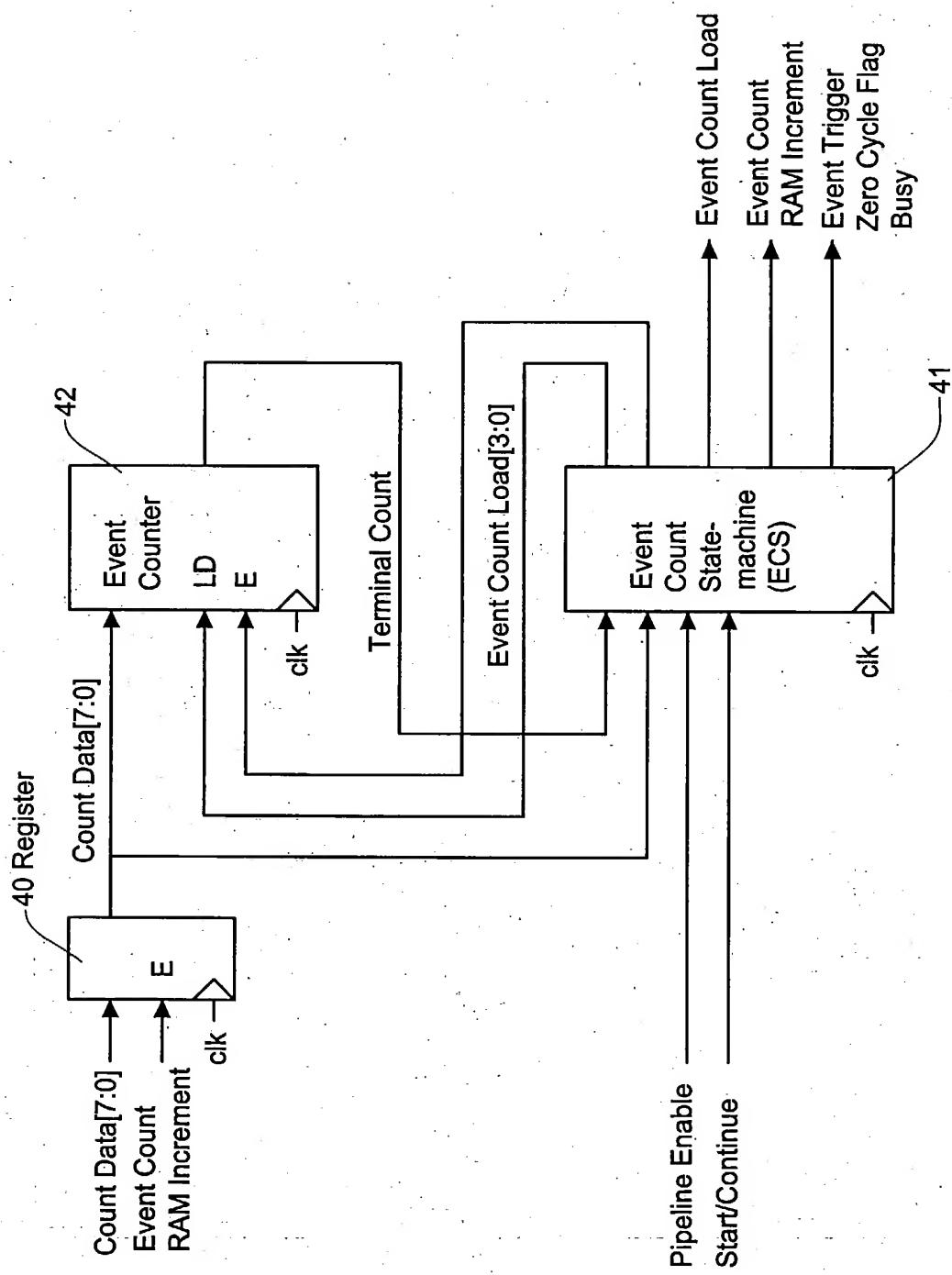


Fig. 8

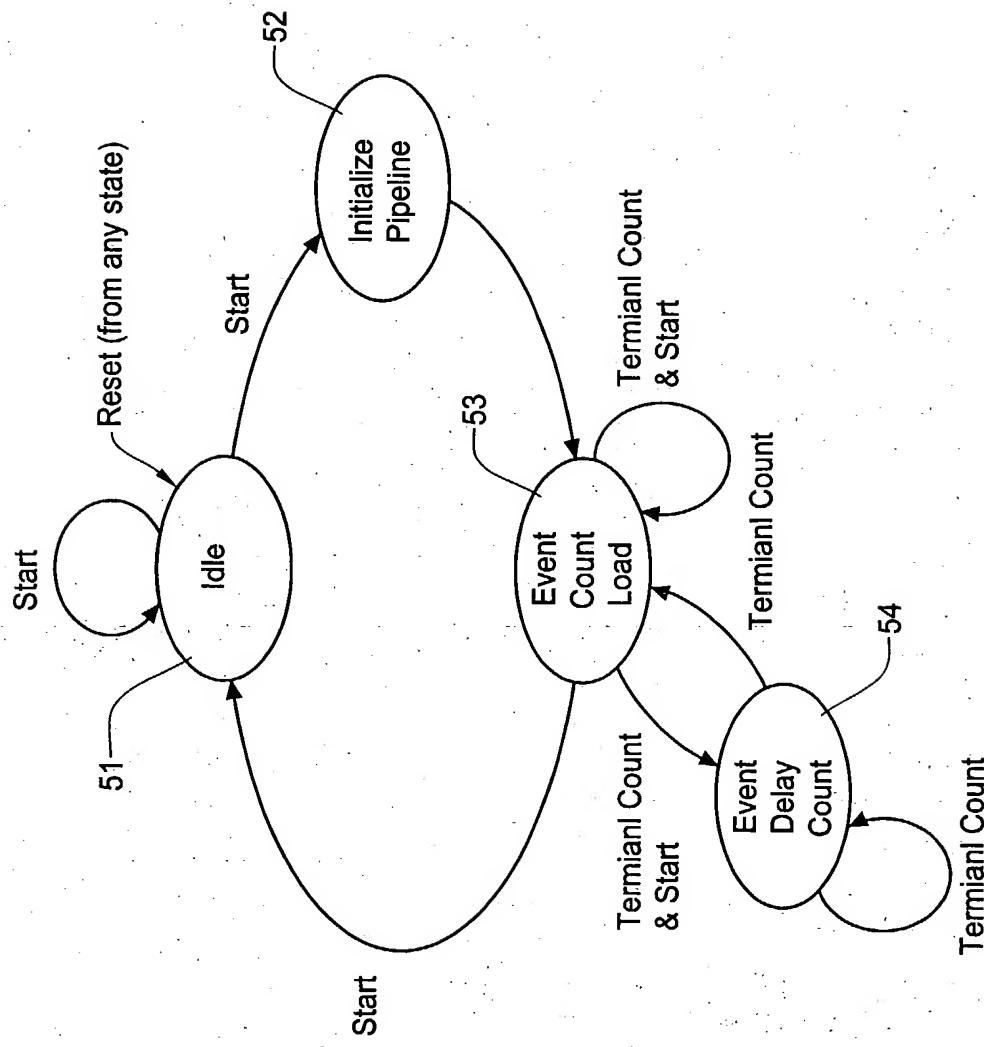


Fig. 9

Address	Bit[7]	Bit[6:5]	Bit[4:0]
Single Word			
N	0	EVCNT[1:0]	COUNT[4:0]
Double Word			
N	0	EVCNT[1:0]	COUNT[4:0]
N+1	1	COUNT[11:10]	COUNT[9:5]
Triple Word			
N	0	EVCNT[1:0]	COUNT[4:0]
N+1	0	COUNT[11:10]	COUNT[9:5]
N+2	1	COUNT[18:17]	COUNT[16:12]
Quad Word			
N	0	EVCNT[1:0]	COUNT[4:0]
N+1	0	COUNT[11:10]	COUNT[9:5]
N+2	0	COUNT[18:17]	COUNT[16:12]
N+3	1	COUNT[25:24]	COUNT[23:19]

Fig. 10

Address	Vernier Pipeline 0	Vernier Pipeline 1	Vernier Pipeline 2	Vernier Pipeline 3
0x0	Event 0, Vernier 0	Event 0, Vernier 1	Event 0, Vernier 2	Event 1, Vernier 0
0x1	Event 1, Vernier 1	Event 1, Vernier 2	Event 1, Vernier 3	Event 2, Vernier 0
0x2	Event 3, Vernier 0	Event 4, Vernier 0	Event 4, Vernier 1	Event 5, Vernier 0
0x3	Event 5, Vernier 1	Event 5, Vernier 2	Event 6, Vernier 0	Event 6, Vernier 1
0x4	Event 7, Vernier 0	Event 7, Vernier 1	Event 8, Vernier 0	Event 9, Vernier 0

Fig. 11

Event Number	EVCNT [1:0]	ECR Address	EVR Address	Vernier Pipeline 0	Vernier Pipeline 1	Vernier Pipeline 2	Vernier Pipeline 3
0	0x2	0x0	0x0	Vernier 0	Vernier 1	Vernier 2	
1	0x3	0x1	0x0-0x1	Vernier 1	Vernier 2	Vernier 3	Vernier 0
2	0x0	0x2	0x1				Vernier 0
3	0x0	0x3	0x2	Vernier 0			
4	0x1	0x4	0x2		Vernier 0	Vernier 1	
5	0x2	0x5	0x2-0x3	Vernier 1	Vernier 2		Vernier 0
6	0x1	0x6	0x3			Vernier 0	Vernier 1
7	0x1	0x7	0x4	Vernier 0	Vernier 1		
8	0x0	0x8	0x4			Vernier 0	
9	0x0	0x9	0x4				Vernier 0

Fig. 12A

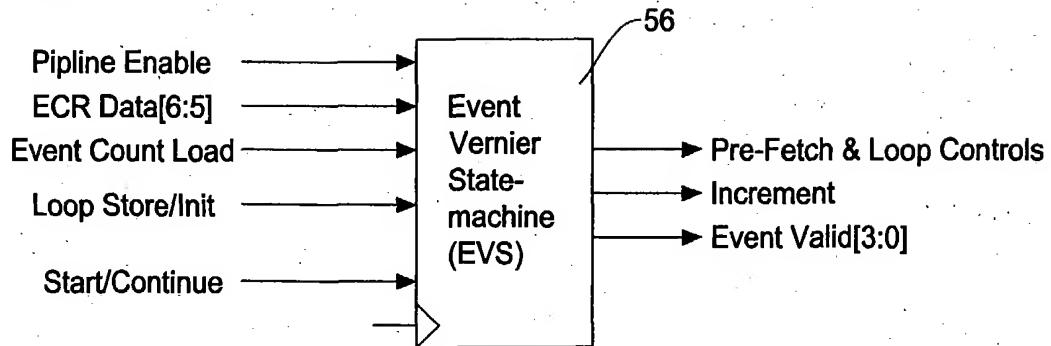


Fig. 12B

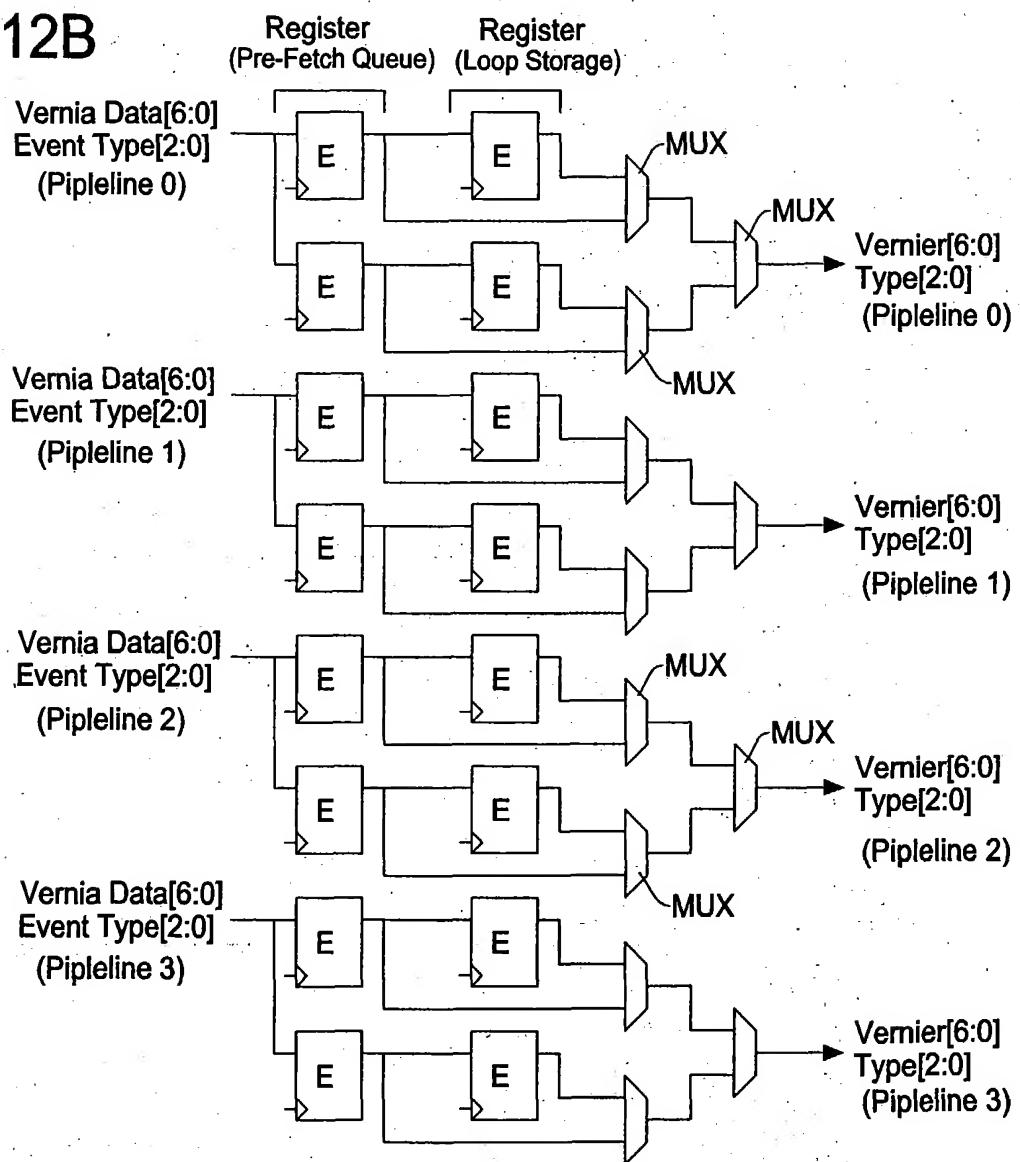


Fig. 13

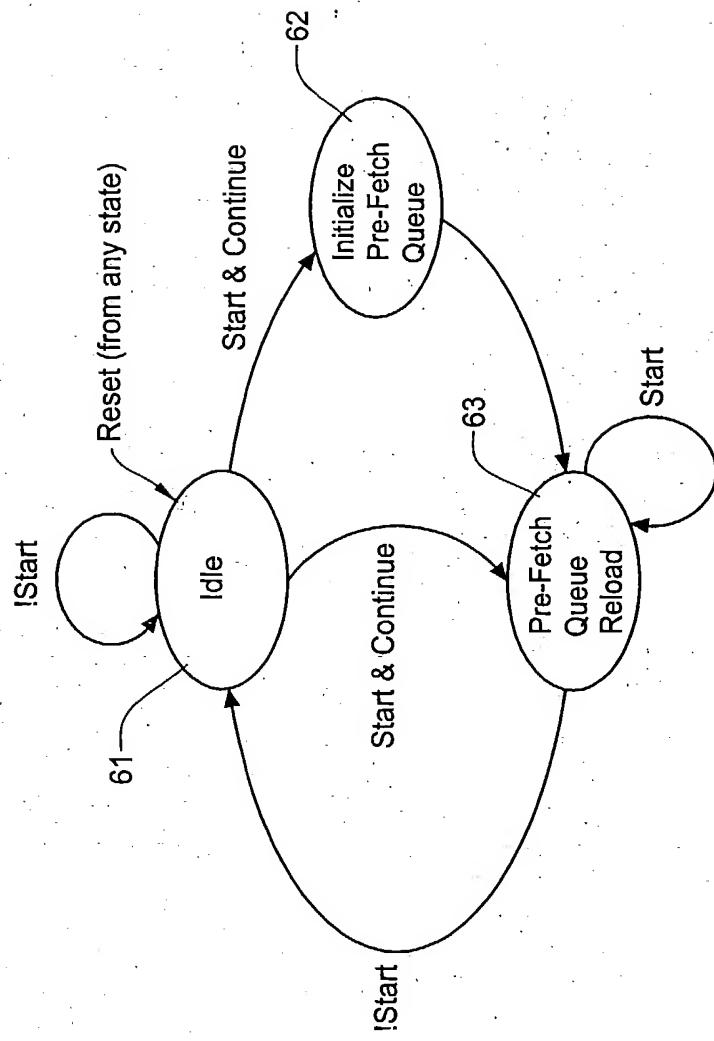


Fig. 14

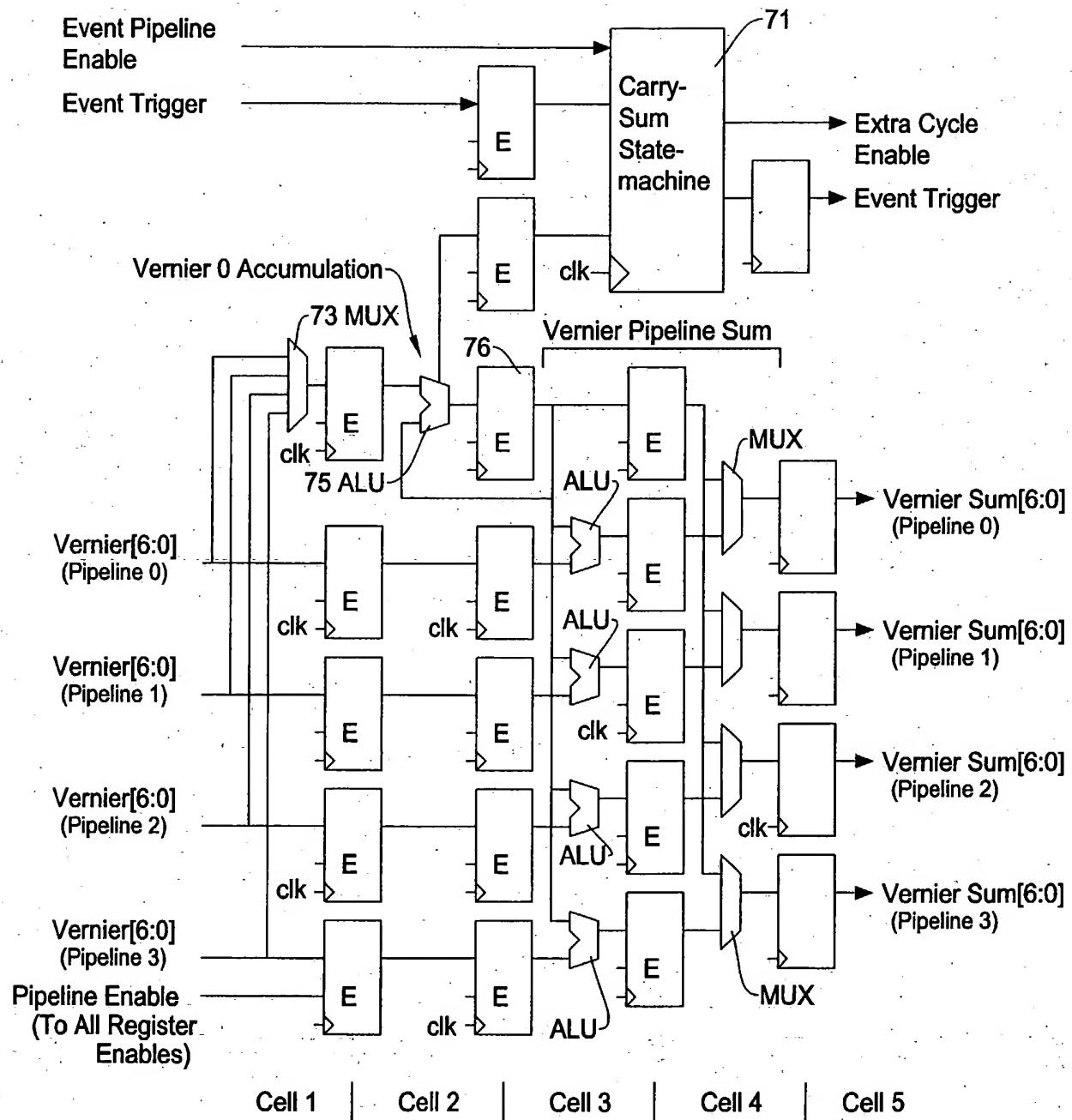


Fig. 15

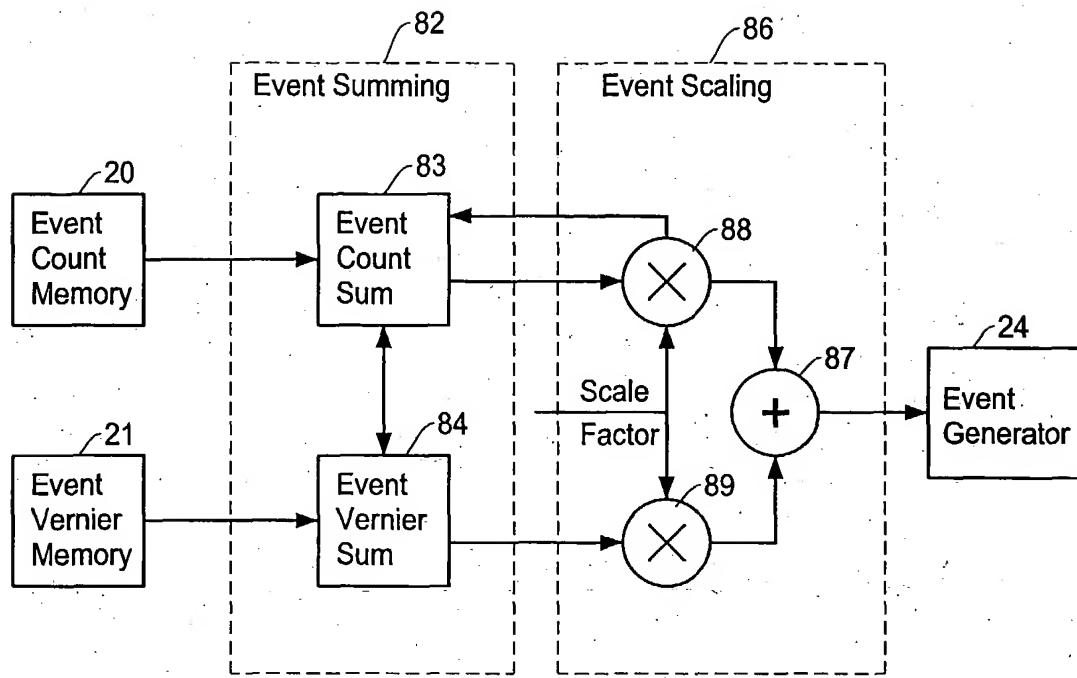


Fig. 16

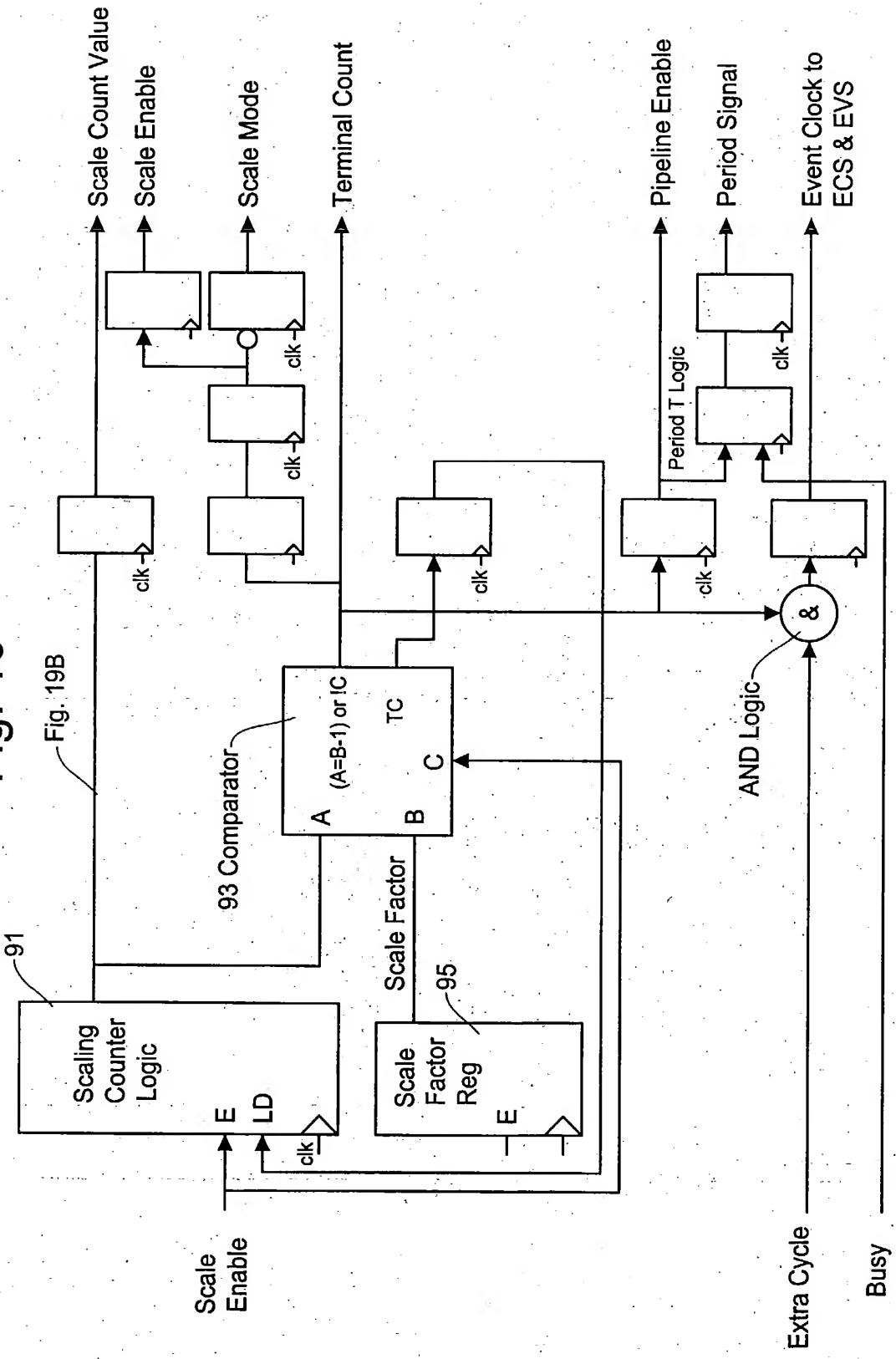


Fig. 17

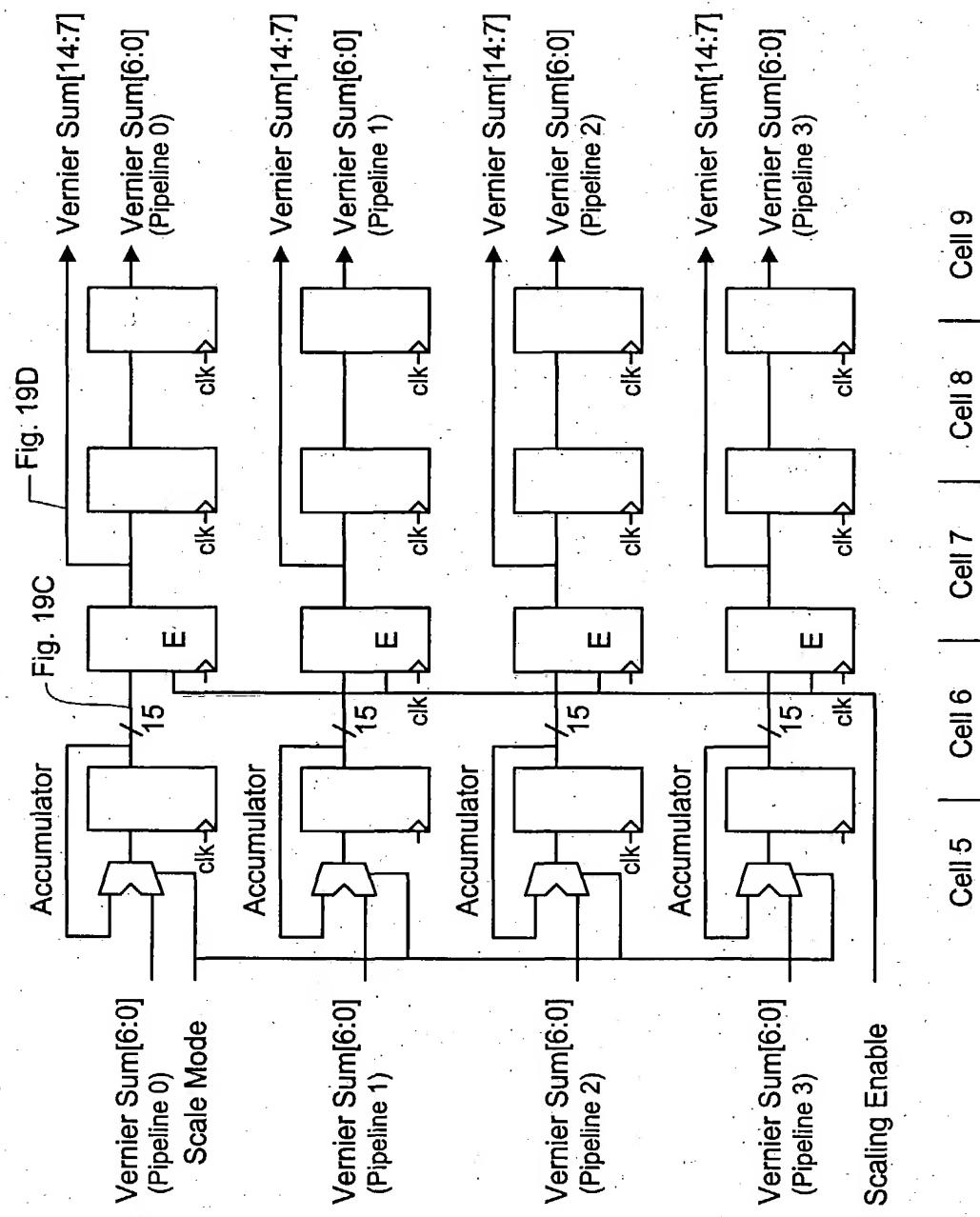


Fig. 18

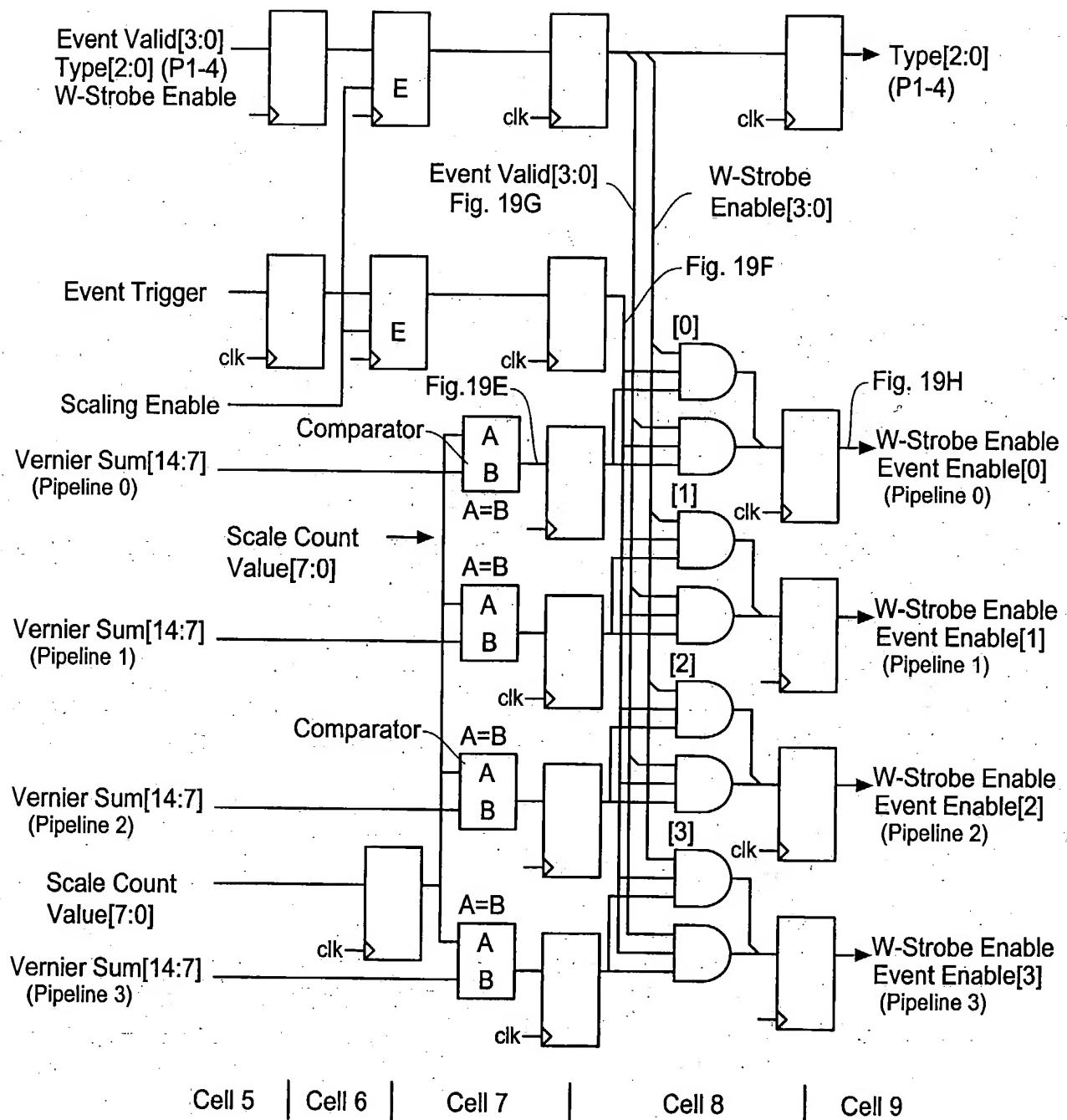


Fig. 19A
Master Clock

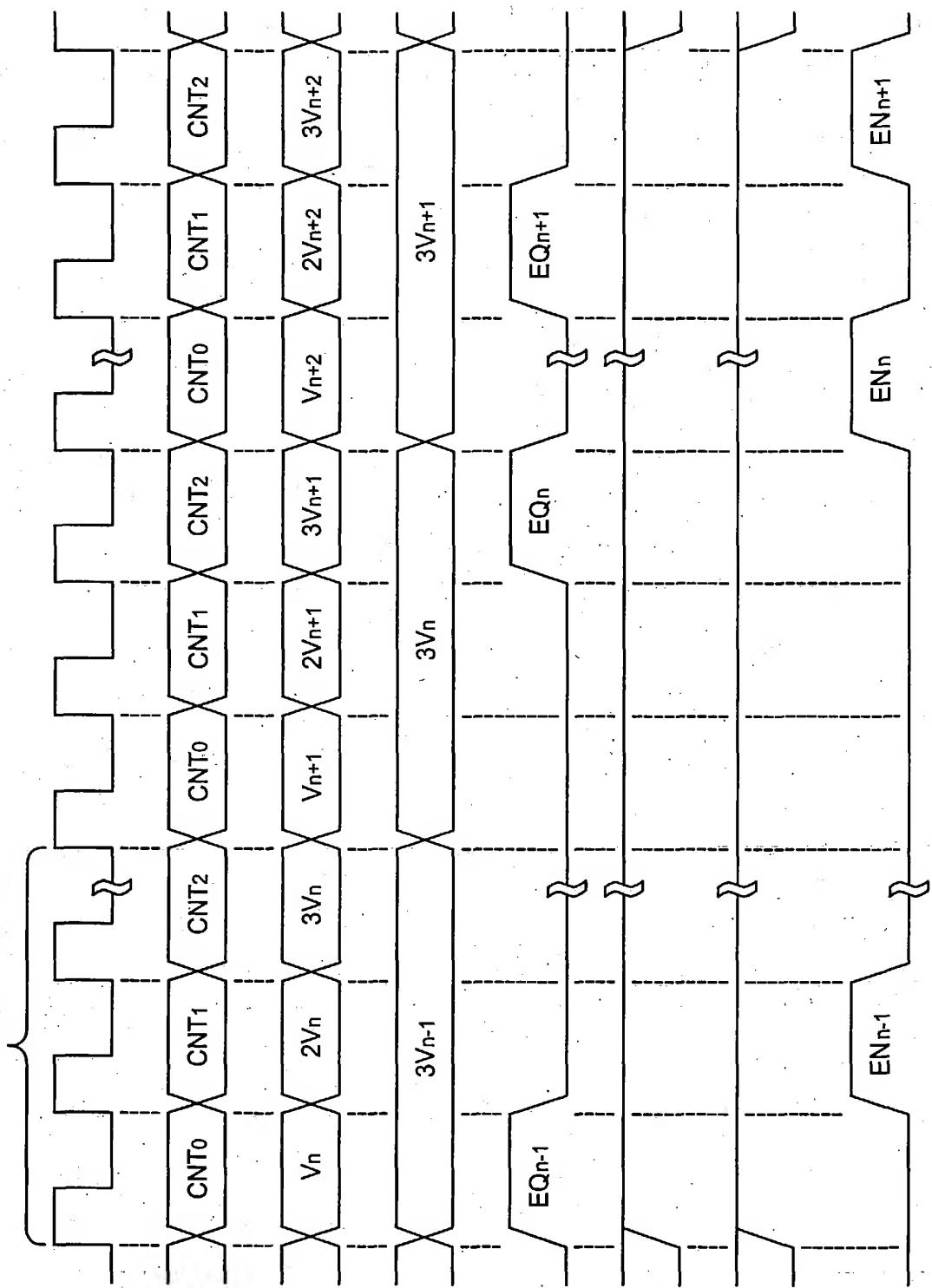


Fig. 19B
Scale Count

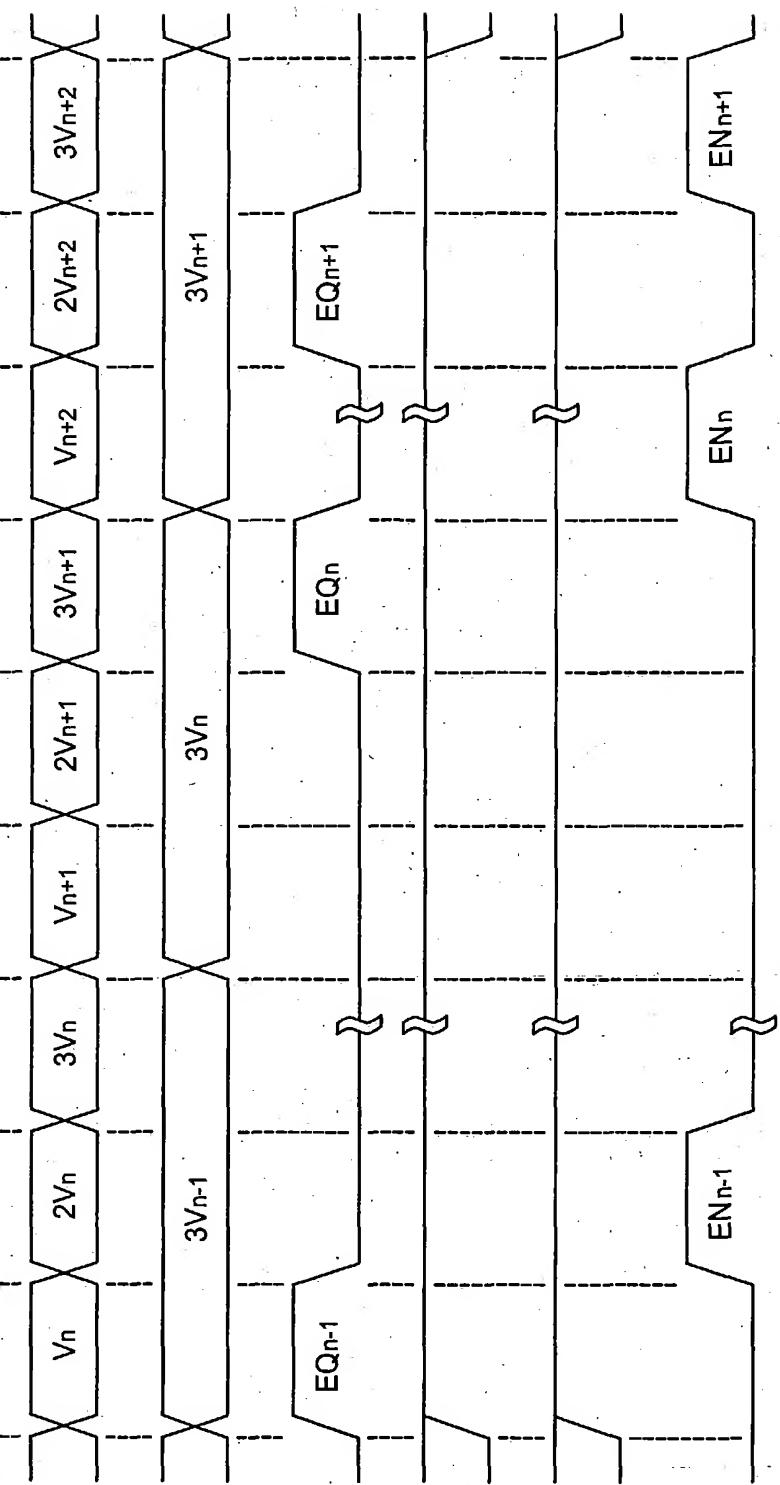


Fig. 19C
Accumulator Out

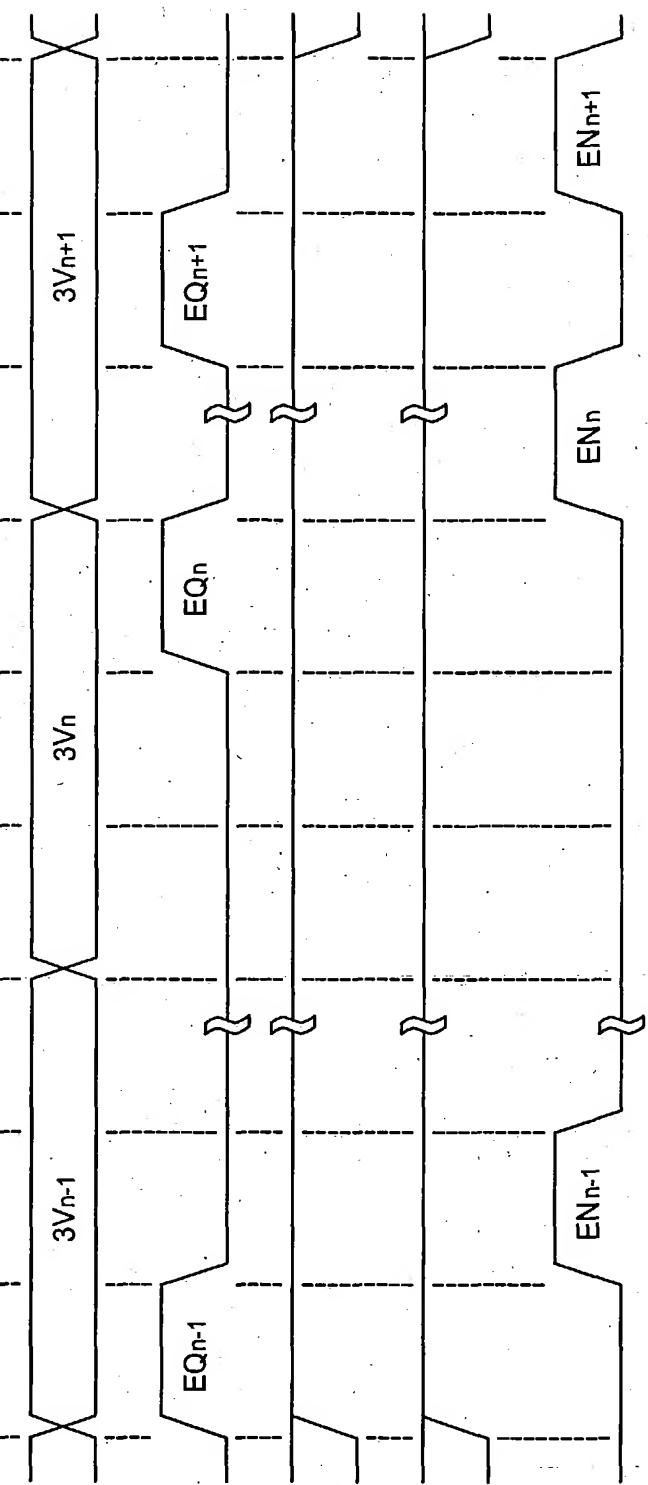


Fig. 19D
Scaled Vernier

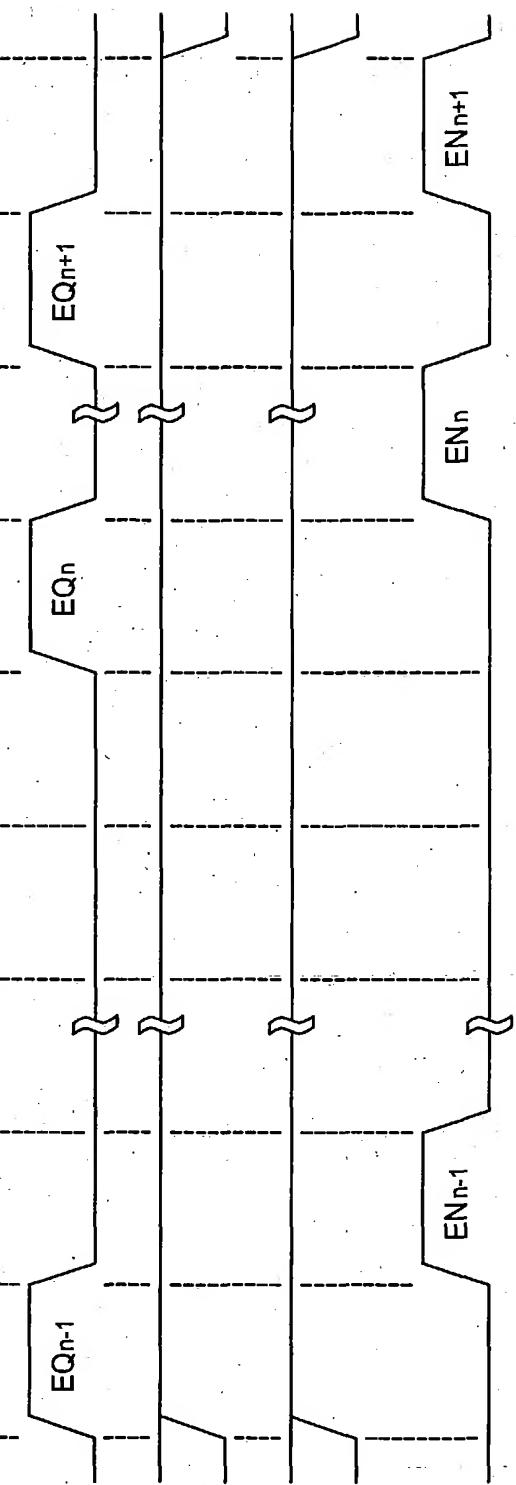


Fig. 19E
Comparator Out

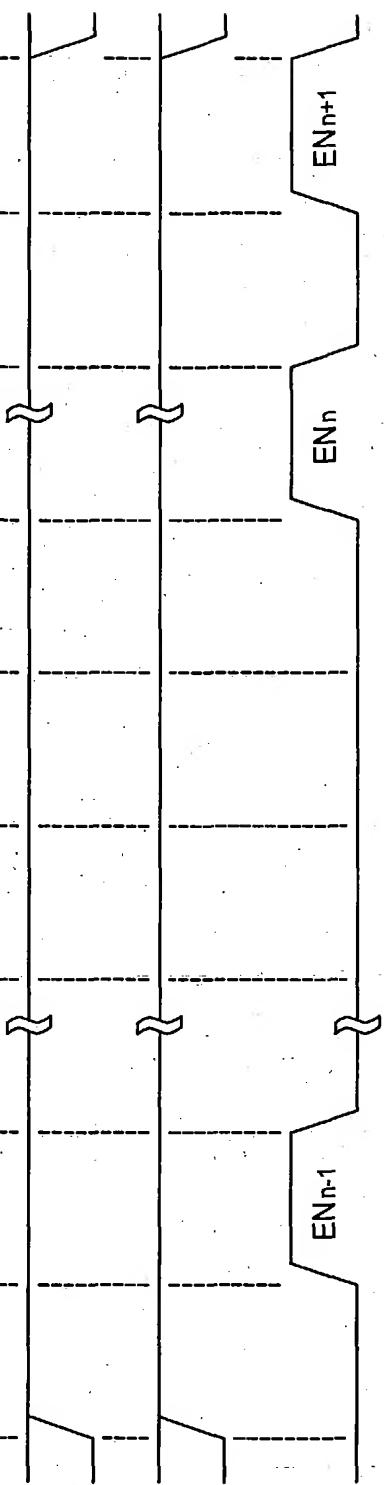


Fig. 19F
Event Trigger

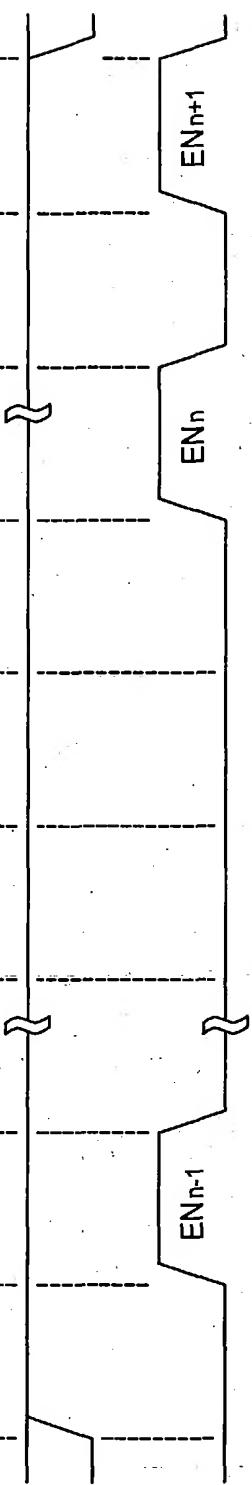


Fig. 19G
Event Valid

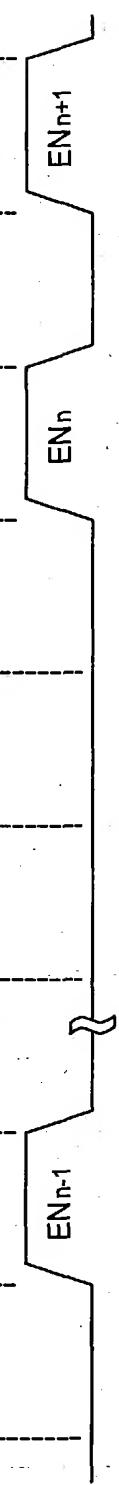


Fig. 19H
Event Enable

Fig. 20A
(Clock)

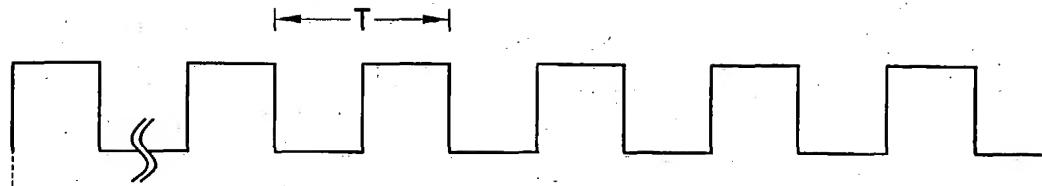


Fig. 20B
(Drive Event)



Fig. 20C
(DUT Out)

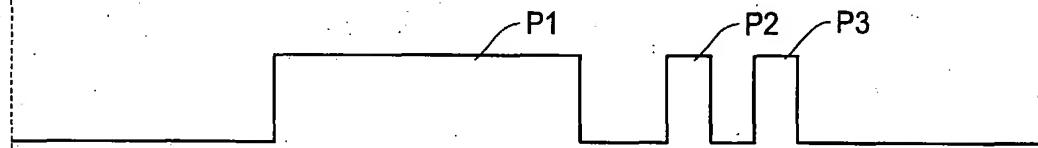


Fig. 20D
(Strobe Event)

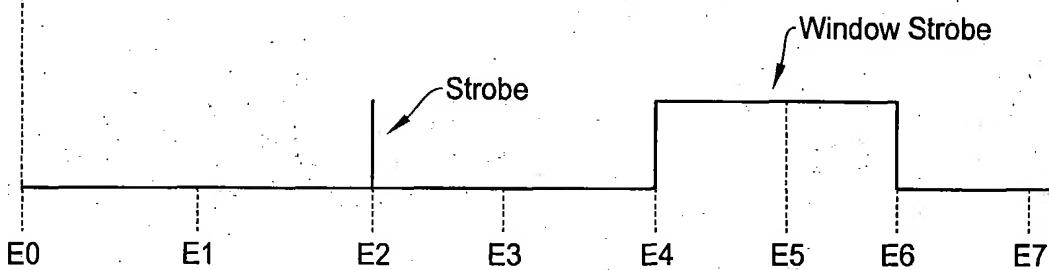


Fig. 21

Event	Event Count	Event Vernier	Event Type
E0	C0	V0	Drive Low
E1	C1	V1	Drive Low
E2	C2	V2	Strobe
E3	C3	V3	Drive Low
E4	C4	V4	Strobe
E5	C5	V5	Strobe
E6	C6	V6	Drive Low
E7	C7	V7	Drive Low

Fig. 22

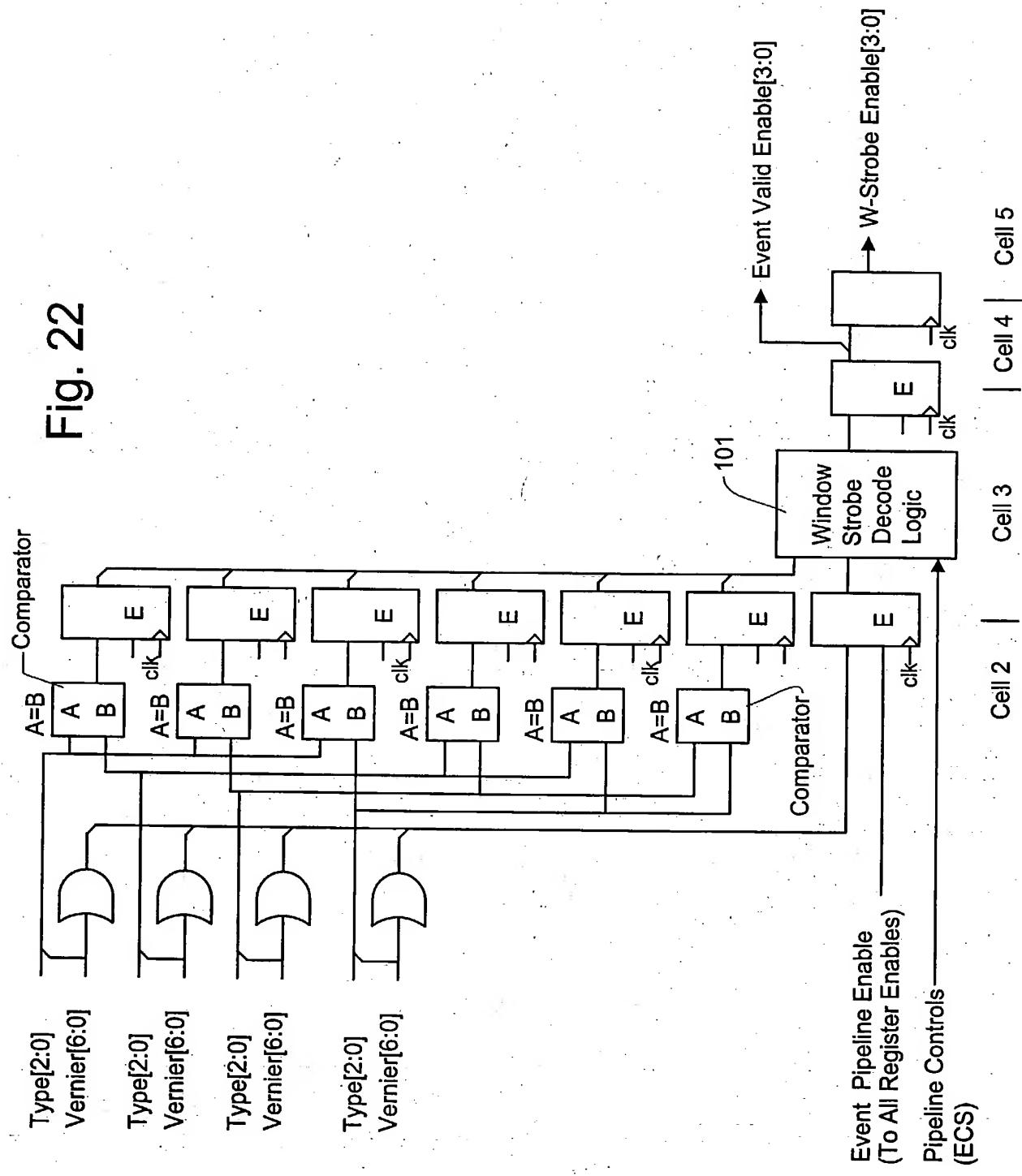


Fig. 23A

Window Strobe Type Comparisons				
	Type 0	Type 1	Type 2	Type 3
Type 0		X	X	X
Type 1	X		X	X
Type 2	X	X		
Type 3	X	X	X	

Fig. 23B

Window Strobe Vernier Comparisons				
	Vernier 0	Vernier 1	Vernier 2	Vernier 3
Vernier 0		X	X	X
Vernier 1	X		X	X
Vernier 2	X	X		
Vernier 3	X	X	X	

Fig. 24A

Window Strobe Determinations for Vernier 0				
	Type 0	Type 1	Type 2	Type 3
Vernier = 0	Type 0		W	W
	Type 1			
	Type 2			
	Type 3			
Vernier ≠ 0	Type 0			
	Type 1			
	Type 2			
	Type 3			

Fig. 24B

Window Strobe Determinations for Verniers 1, 2, and 3				
	Type 0	Type 1	Type 2	Type 3
Matching Verniers	Type 0			
	Type 1			W
	Type 2	W		W
	Type 3	W	W	
No Matching Verniers	Type 0			
	Type 1			
	Type 2			
	Type 3			

Fig. 25

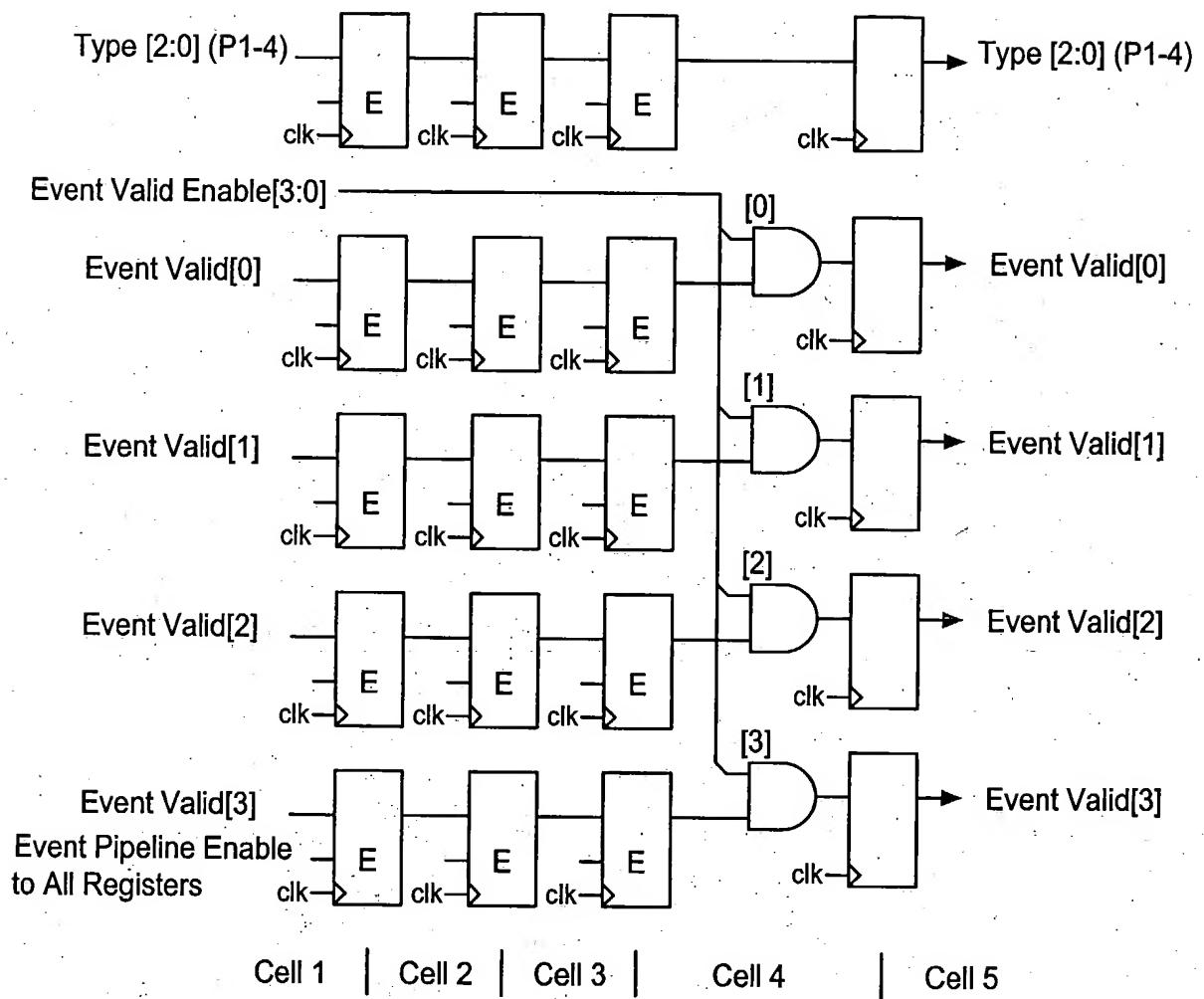


Fig. 26

Window Strobe Event Type Removals				
	Type 0	Type 1	Type 2	Type 3
Vernier = 0	Type 0		Type 1	Type 2
	Type 1			
	Type 2			
	Type 3			
Vernier \neq 0	Type 0			
	Type 1			
	Type 2			
	Type 3			
Matching Verniers	Type 0			
	Type 1			Type 2
	Type 2		Type 1	Type 3
	Type 3		Type 1	Type 3
No Matching Verniers	Type 0			
	Type 1			
	Type 2			
	Type 3			

Fig. 27A

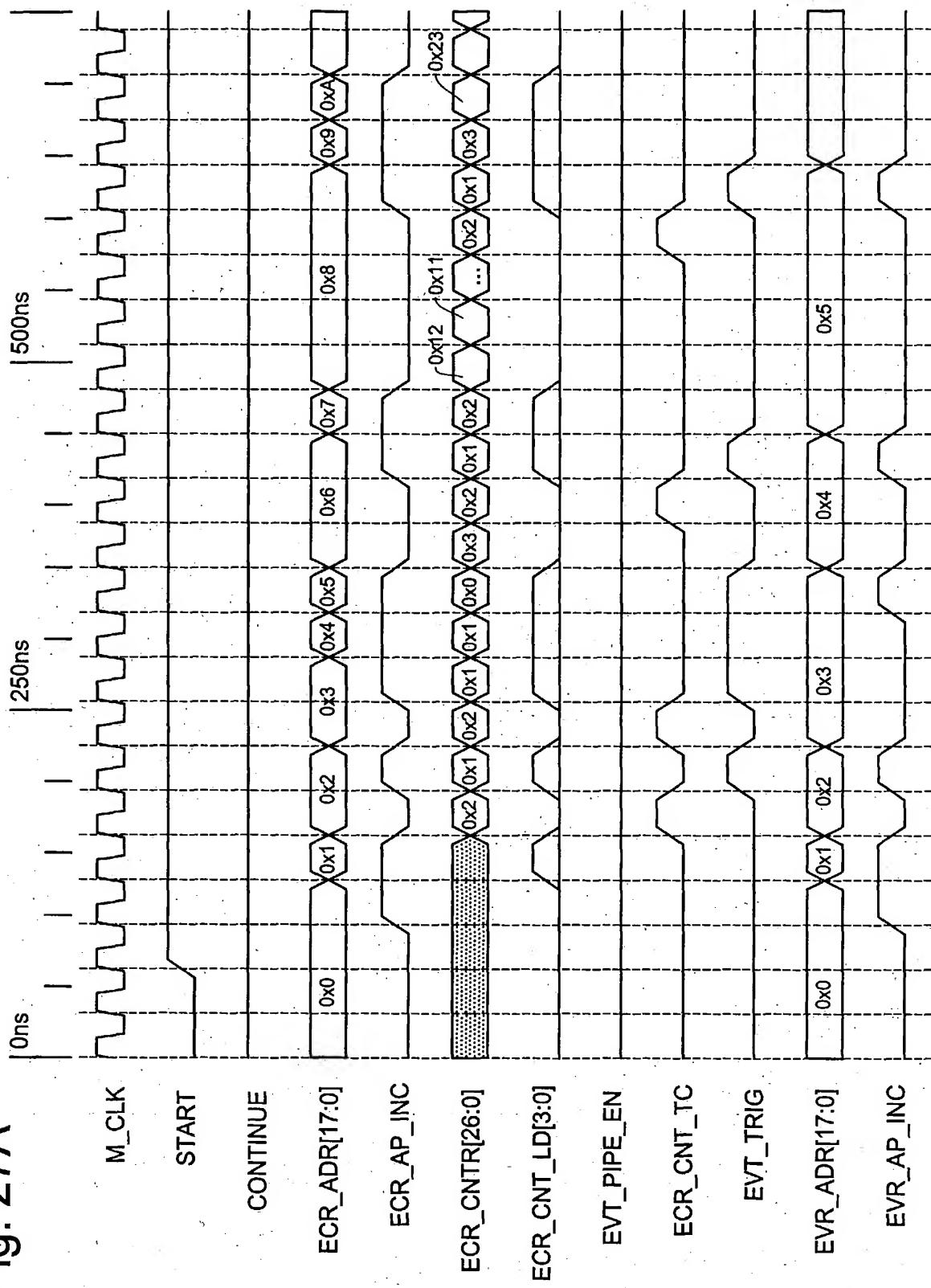


Fig. 27B

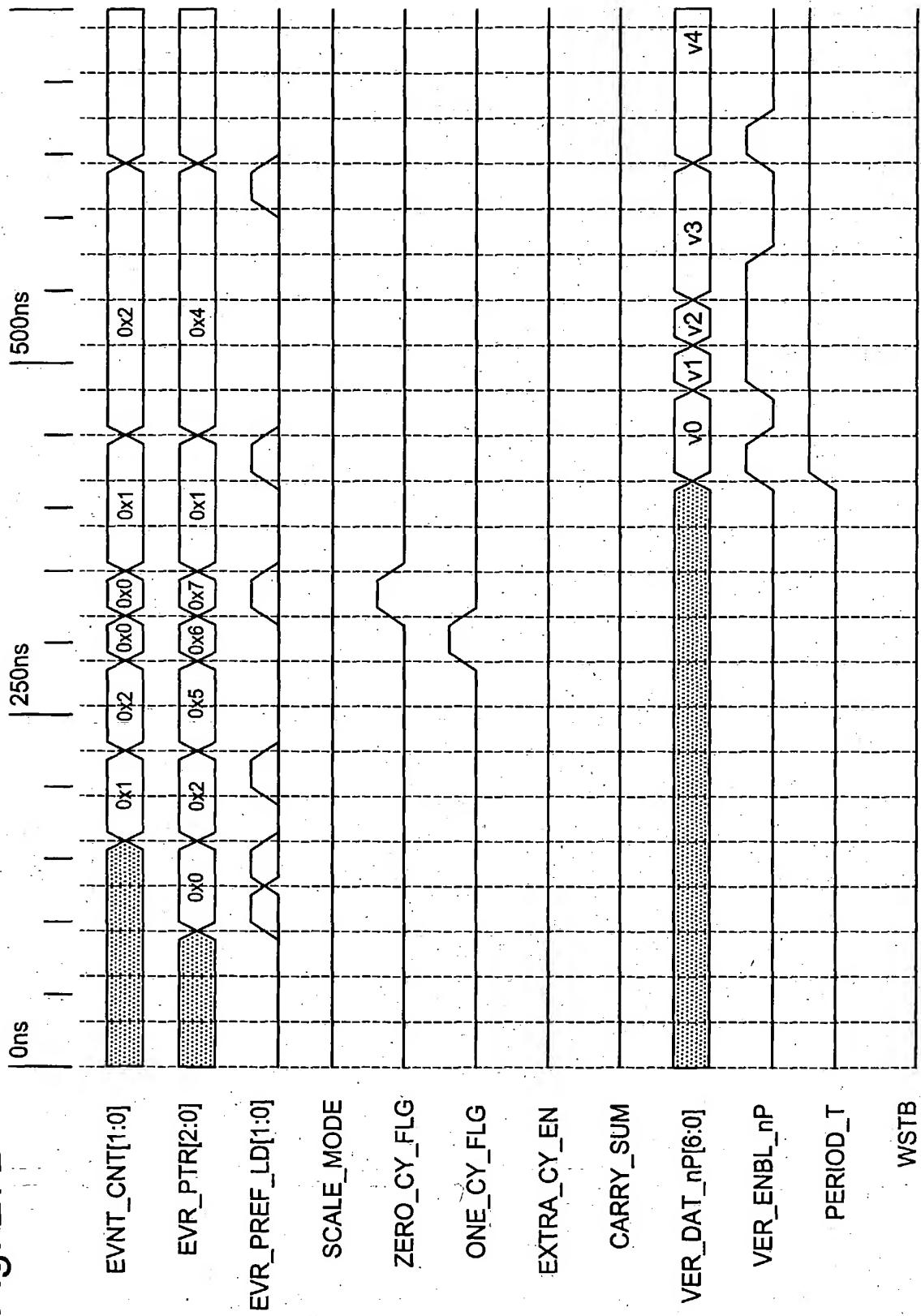


Fig. 28A

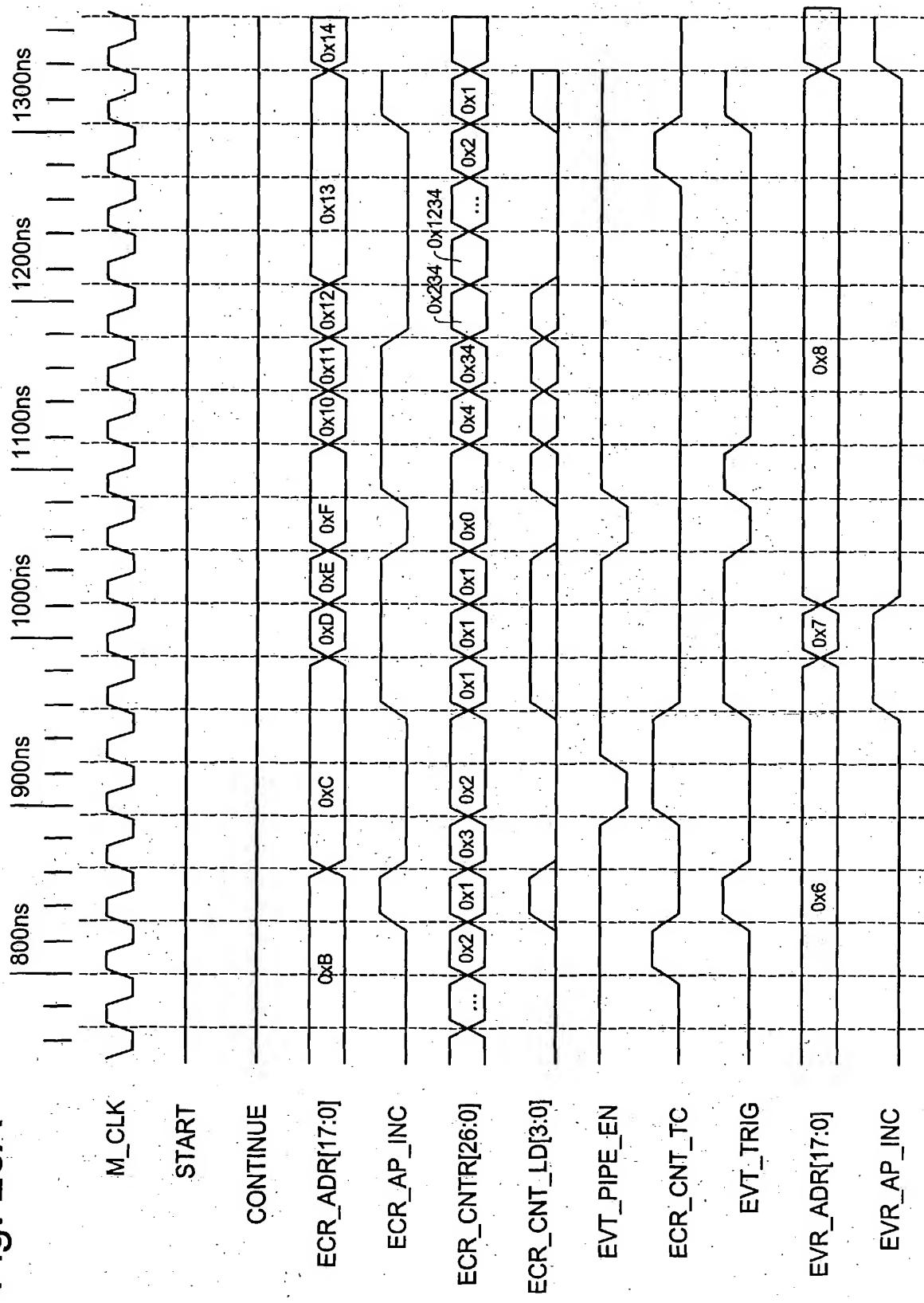


Fig. 28B

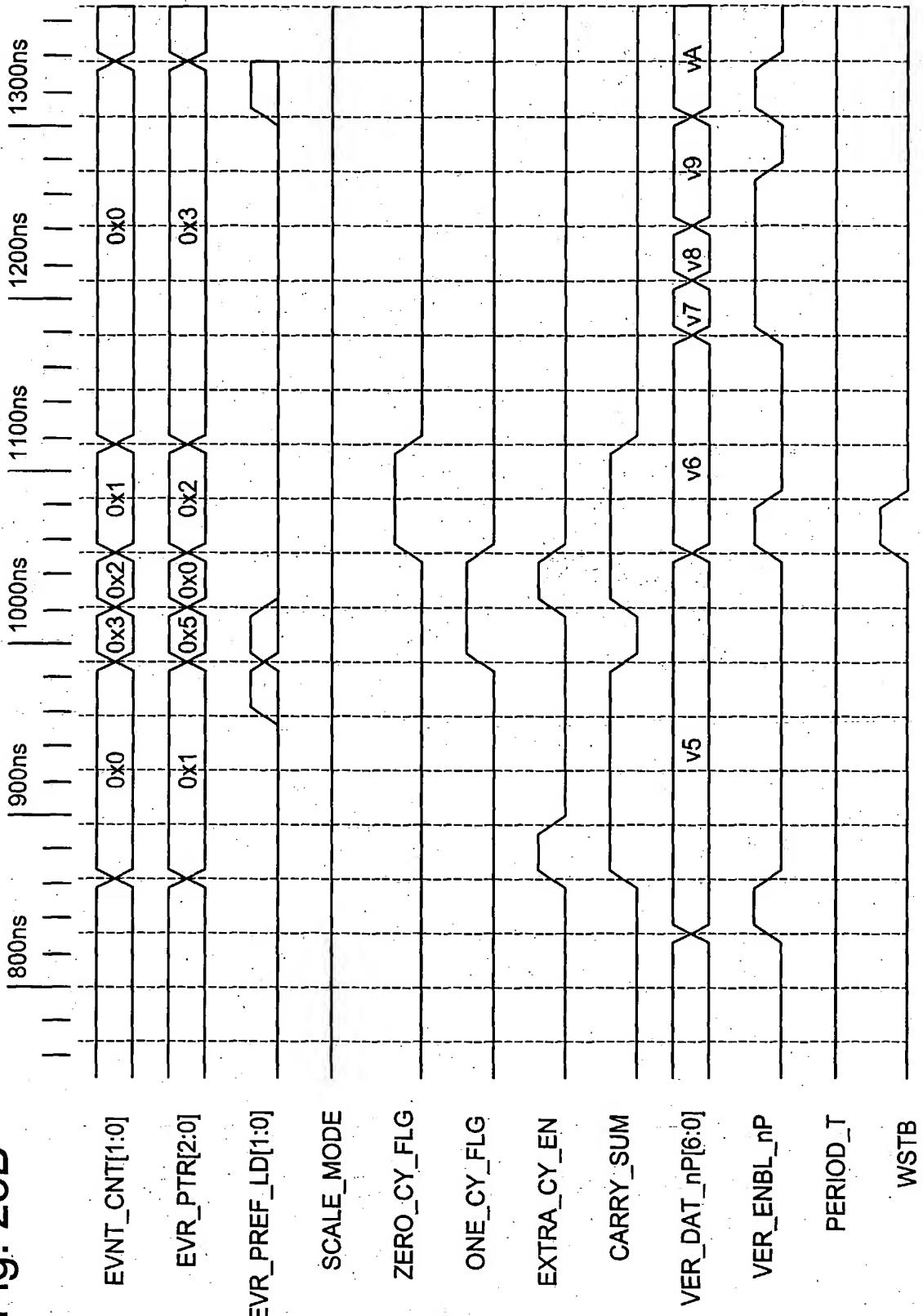


Fig. 29A

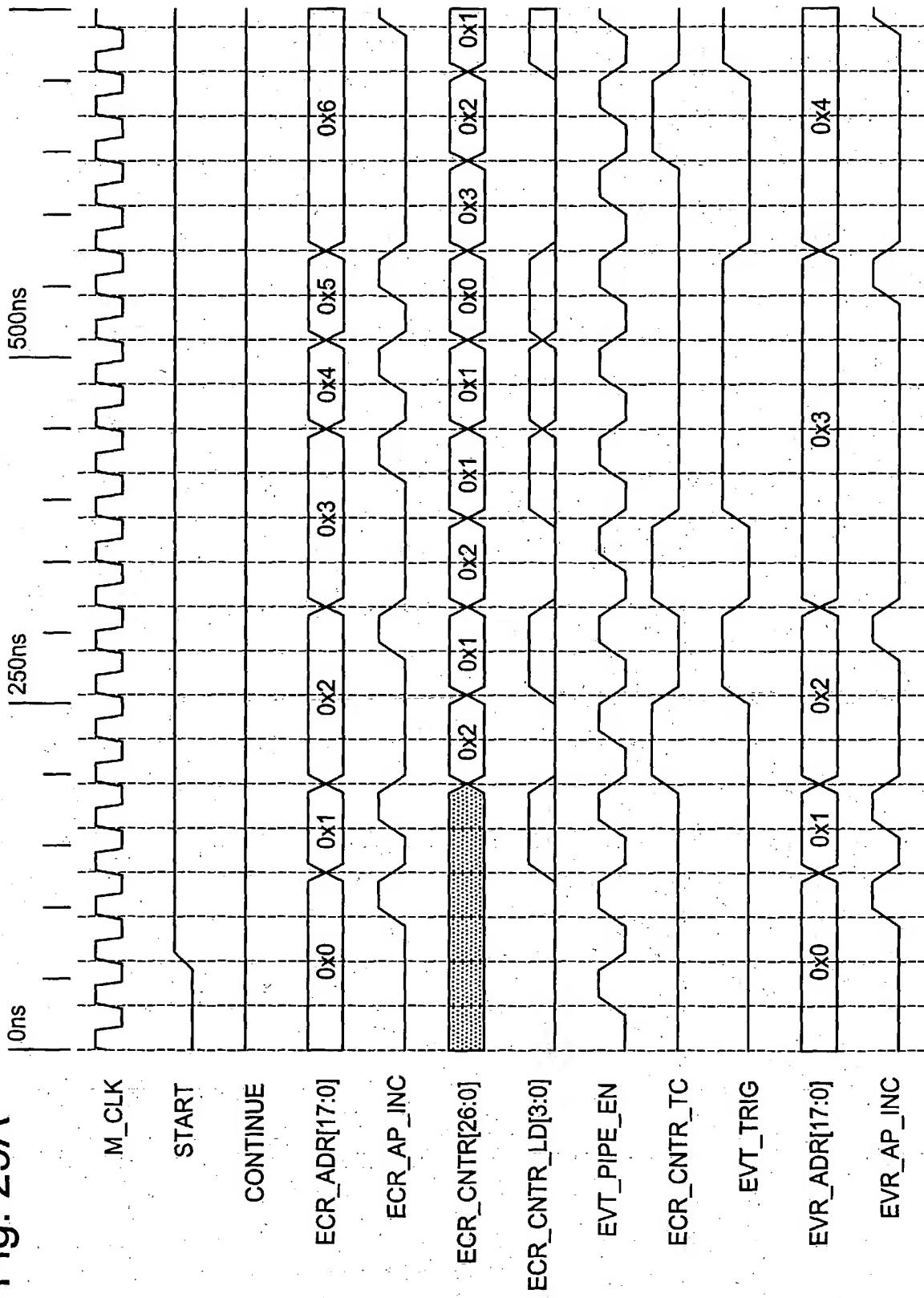


Fig. 29B

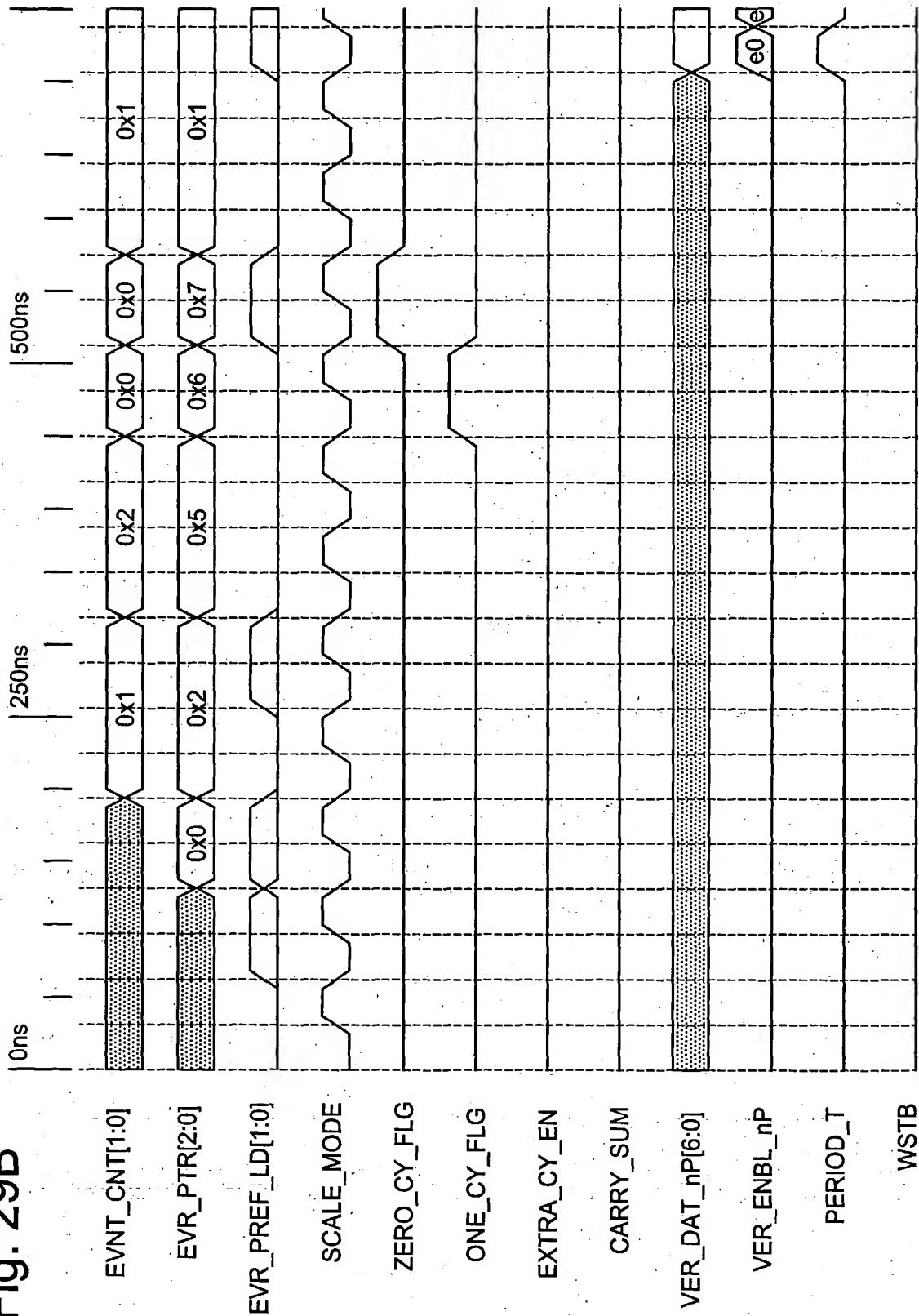


Fig. 30A

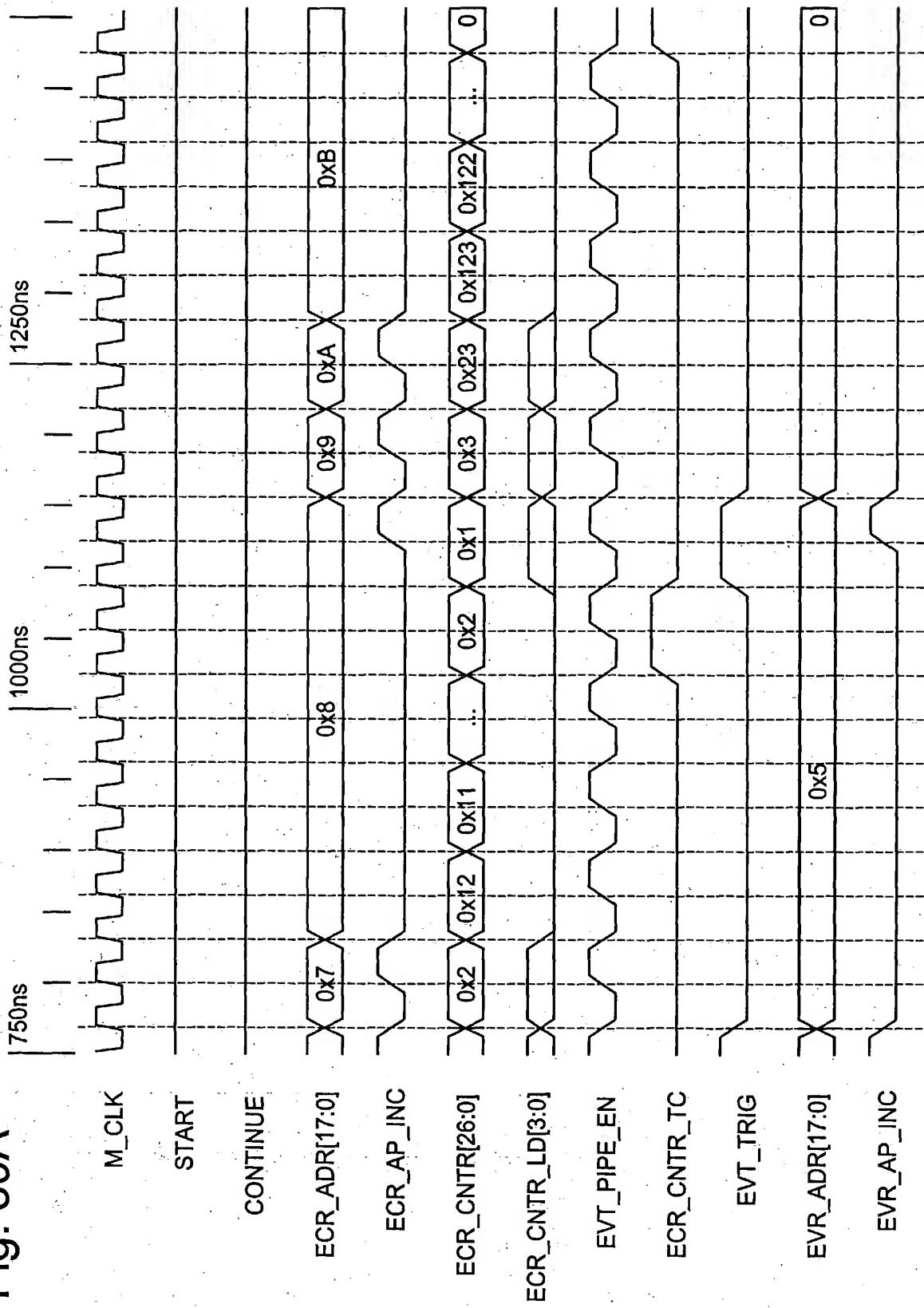


Fig. 30B

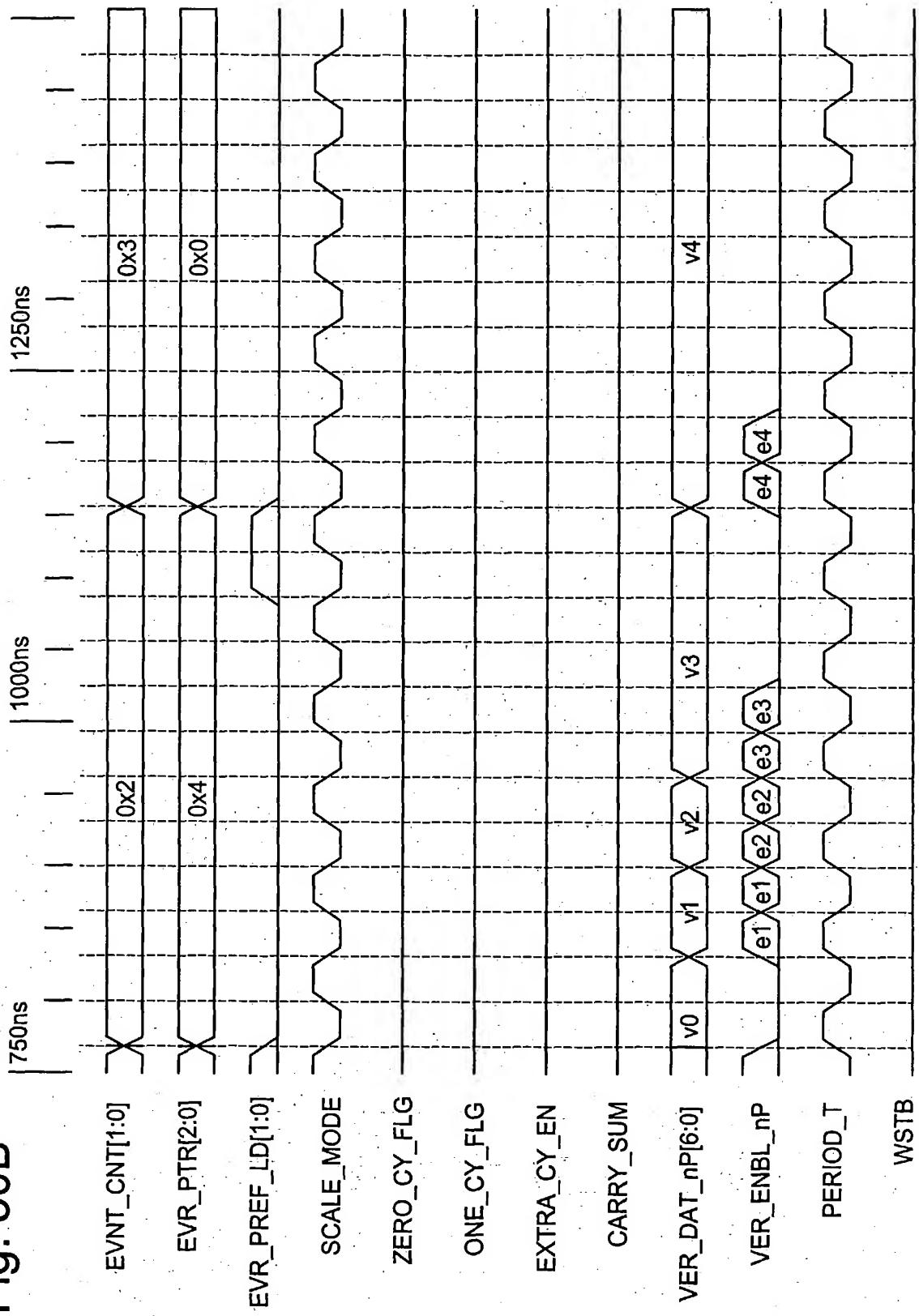


Fig. 31A

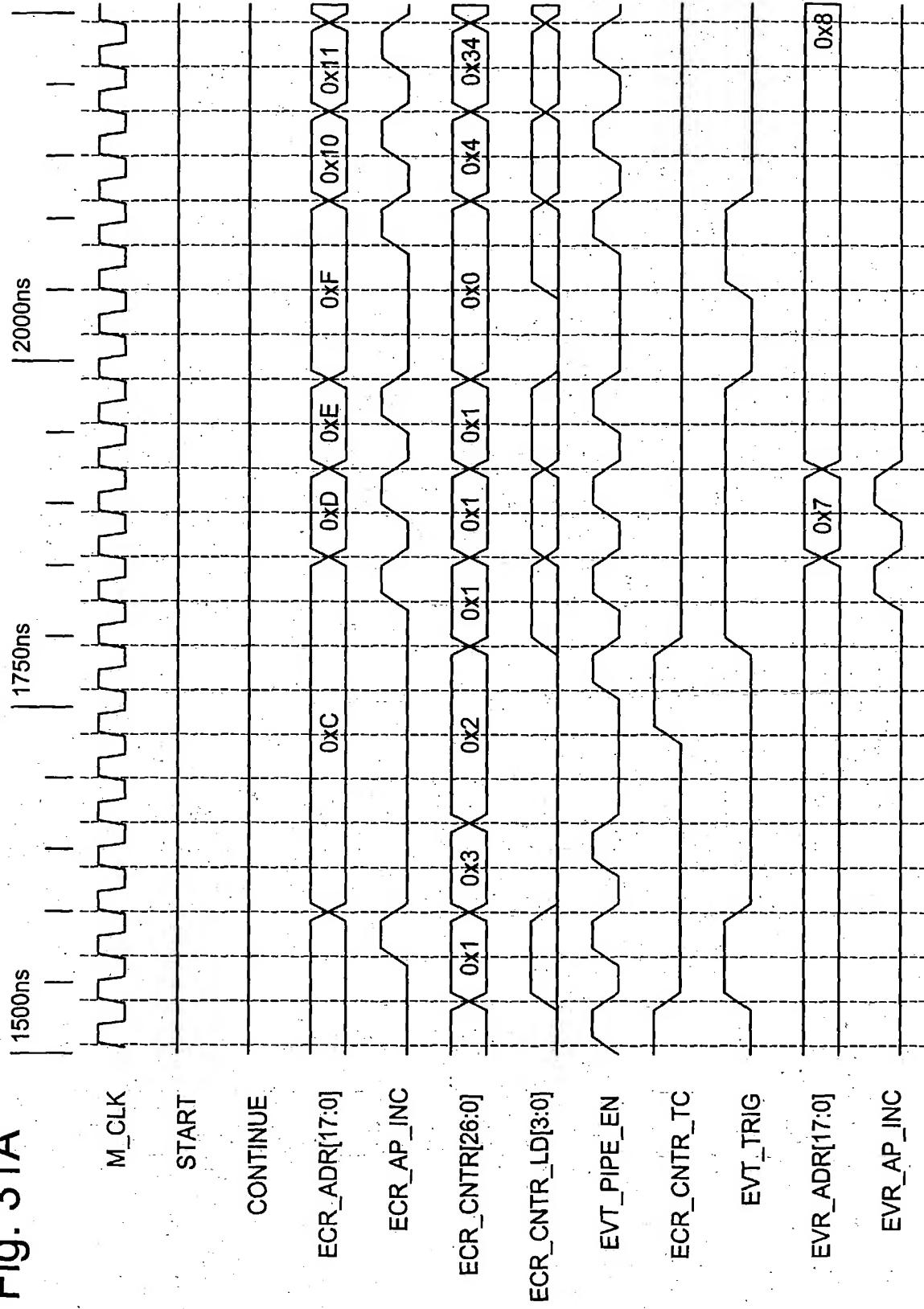


Fig. 31B

